Synopsys and TSMC Collaborate for 20nm Reference Flow

Design Tools Selected in Reference Flow for Physical Implementation, RC Extraction, Timing Analysis and Physical Verification

MOUNTAIN VIEW, Calif., Oct. 15, 2012 /PRNewswire/ --

Highlights:

- TSMC 20nm Reference Flow deployed by early adopters for design enablement
- Flow provides proven support for double patterning, pre-coloring, pattern matching, multi-valued SPEF
- Flow includes Synopsys' Design Compiler®, IC Compiler™, StarRC™, PrimeTime® and IC Validator tools

Synopsys, Inc. (Nasdaq: SNPS), a global leader accelerating innovation in the design, verification and manufacture of chips and systems, today announced 20-nanometer (nm) process technology support for the TSMC 20nm Reference flow. This includes Synopsys® Galaxy™ Implementation Platform support for the latest TSMC 20nm design rules and models. The collaboration between TSMC and Synopsys on 20nm technology allows designers to gain performance, power efficiency and chip density advantages while achieving predictable design closure with the industry-proven Synopsys RTL to GDSII solution.

TSMC's 20nm Reference Flow addresses 20nm design challenges with a transparent double patterning aware design flow enabling double patterning technology (DPT) compliance, pre-coloring capability, new RC extraction methodology, DPT sign-off, and integrated design-for-manufacturing (DFM). The new Reference Flow's transparent DPT enablement reduces DPT design complexity, achieves required accuracy, minimizes 20nm design flow setup and learning curve, and accelerates 20nm process adoption.

"The 20nm process offers measurable power, performance and area benefits. However, it brings with it new design challenges, including double patterning," said Antun Domic, senior vice president and general manager of the implementation group at Synopsys. "TSMC and Synopsys have collaborated closely from the very early stages of 20-nanometer process development to address these challenges. The results of this collaboration will help designers maximize the benefits of the 20-nanometer process to deliver their designs predictably and on time."

"Synopsys and TSMC have a successful track record of collaborating to maximize the benefits of new TSMC process technology and Synopsys EDA tool support for our mutual customers," said Suk Lee, TSMC Senior Director, Design Infrastructure Marketing Division. "Delivery of the 20nm Reference Flow is the latest example of this technology partnership."

About Synopsys Support for the TSMC 20nm Reference Flow and Certification Program

Synopsys' Galaxy Implementation Platform supports TSMC's 20nm process. Supported tools include:

- **IC Compiler:** Offers industry's leading solution for power, performance and area on advanced node designs, and enables designers to create DPT compliant layout that can be reliably decomposed during manufacturing
- **IC Validator:** Features a fast, accurate decomposition (coloring engine) to perform double-patterning checks during design, and can also perform automatic fixing of violations with IC Compiler via In-Design technology
- **PrimeTime:** Enables double-patterning-aware variation analysis that includes multi-valued SPEF model variation and its impact on timing
- **StarRC:** Provides silicon-calibrated modeling to account for mask misalignment due to double patterning and non-color and color-aware extraction for accurate, high-performance design

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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