TSMC Awards Synopsys "Partner of the Year 2012"

Recognizes Synopsys' Valuable Contributions towards Development of 20-nm Technology

MOUNTAIN VIEW, Calif., Oct. 17, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that TSMC has awarded Synopsys "Partner of the Year 2012" for joint delivery of TSMC 20-nanometer Reference Flow. The award recognizes Synopsys' broad and deep technical expertise and shared commitment to the development and delivery of TSMC's 20nm reference flow. The Synopsys solution for this flow includes the Design Compiler®, IC Compiler™, StarRC™, PrimeTime® and IC Validator tools.

"By making insightful R&D contributions and engaging with a broad solution, Synopsys has significantly advanced development and deployment of 20-nanometer process technology," said Suk Lee, TSMC Senior Director of Design Infrastructure Marketing Division. "We are pleased to give the Partner of the Year 2012 award to Synopsys and look forward to working together to bring more innovations to the field of semiconductor design."

"We are honored to receive this prestigious award from TSMC," said John Chilton, senior vice president marketing and business development at Synopsys. "Our mutual customers demand the best from process and EDA tools and IP to meet their aggressive market needs. Through this kind of deep collaboration with our partners, we continue to advance the state-of-the-art for design engineers."

About Synopsys Support for the TSMC 20nm Reference Flow

Synopsys' Galaxy™ Implementation Platform supports TSMC's 20nm process:

- **IC Compiler:** Offers the industry's leading solution for power, performance and area on advanced node designs, and enables designers to create a DPT-compliant layout that can be reliably decomposed during manufacturing.
- **IC Validator:** Features a fast, accurate decomposition (coloring engine) to perform 20-nm rule checks, including DPT, during design and can also perform automatic fixing of violations with IC Compiler through In-Design technology.
- **PrimeTime:** Enables DPT-aware variation analysis that includes multi-valued SPEF model variation and its impact on timing.
- **StarRC:** Provides silicon-calibrated modeling to account for mask misalignment due to double patterning as well as non-color and color-aware extraction for accurate, high-performance design.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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