UMC Qualifies Synopsys' IC Validator for 28-nm Physical Verification

UMC Qualification Brings More Process and Foundry Choices to IC Compiler and IC Validator User Base

MOUNTAIN VIEW, Calif., Oct. 22, 2012 /PRNewswire/ --

Highlights:

- IC Validator brings In-Design physical verification to designers working at UMC's 28nm node
- In-Design physical verification eliminates late-stage design surprises and manual fixes
- Sign-off accurate Design Rule Checking (DRC) and layout-vs.-schematic (LVS) runsets now available for UMC customers

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Synopsys' IC Validator physical verification product has been qualified by United Microelectronics Corporation for 28-nm physical signoff, with immediate availability of design rule checking (DRC) and layout-vs.-schematic (LVS) runsets to UMC customers. IC Validator, part of the Galaxy™ Implementation Platform, is the ideal add-on to IC Compiler™ for in-design physical verification, making it possible for place-and-route engineers to accelerate time to tapeout by eliminating late-stage surprises and manual fixes. IC Validator is being actively used at process nodes ranging from 65nm to 20nm. UMC's qualification of IC Validator brings the unique benefits of in-design physical verification to design teams working at UMC's 28-nm process node.

"UMC is committed to making available to its customers solutions that ensure silicon success while optimizing design turnaround time. As such, optimal runset creation and efficient maintenance are of paramount importance," said SC Chien, vice president of Customer Engineering& IP Development Design Support at UMC. "Runset creation with IC Validator was completed in record time for our 28-nanometer process node. In addition, our IC Compiler customers can now take advantage of the productivity benefits of In-Design physical verification for faster design closure."

As feature geometries shrink, the number and complexity of DRCs needed to achieve manufacturing compliance is growing exponentially. IC Validator makes runset creation and maintenance effortless for users by providing a hybrid engine for processing checks based on both polygon and edge data. Hybrid processing allows for efficient resolution of dependencies and more intelligent multi-core distribution, yielding faster runtimes. Furthermore, IC Validator enables coding at higher levels of abstraction, streamlining tedious lower-level data processing. Finally, IC Validator is architected for near-linear performance scalability that maximizes utilization of mainstream hardware, using smart, memory-aware load scheduling and balancing technologies.

Traditional physical verification done after design closure is no longer adequate for complex designs, causing late-stage surprises and leading to an increasing number of time-consuming and error-prone design iterations. In-Design physical verification, based on intelligent integration between IC Validator and IC Compiler, makes it possible for place-and-route engineers to perform independent signoff-quality analysis earlier, before the design is finalized and while correction can be automated. In-Design technology enables new high-productivity functionality, such as automatic DRC repair, timing-aware metal fill and rapid ECO validation, all within the place-and-route environment. In-Design physical verification eliminates entire iterations with downstream analysis tools and maintains convergent design evolution to physical signoff.

"As manufacturing complexity places increased pressure on our customers to deliver within schedule, it is important that we continue to collaborate closely with leading foundries like UMC," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "This qualification brings the proven benefits of IC Validator and In-Design physical verification to UMC's customers working at advanced nodes."

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.