New FPGA-Based Prototyping Solution Delivers Up To 3x System Performance Improvement

Synopsys' HAPS-70 Series' Scalable Architecture and Integrated Hardware/Software Prototyping Flow Accelerate Throughput While Increasing Prototyping Capacity to 144 Million ASIC Gates

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Highlights:

- Up to 3x improvement in system prototype performance enabled through enhanced HapsTrak® 3 I/O connector technology and high-speed time-domain multiplexing
- Modular system architecture scales from 12 to 144 Million ASIC gates to accommodate a range of design sizes from individual IP blocks to processor subsystems to complete SoCs
- New capability in Synopsys' Certify® software, in combination with HAPS' flexible interconnect architecture, accelerates multi-FPGA partitioning productivity by up to 10x
- Enhanced Universal Multi-Resource Bus host connectivity of up to 400 MB/s facilitates debug and increases hybrid prototyping performance with Synopsys' Virtualizer™
- Pre-validated Synopsys DesignWare® IP with HAPS systems enables efficient integration of IP blocks and earlier software development

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of Synopsys' HAPS®-70 Series FPGA-based prototyping systems, extending its HAPS product line to address the increasing size and complexity of system-on-chip (SoC) designs. The HAPS-70 systems provide tightly integrated prototyping software and hardware, including high-speed time-domain multiplexing (HSTDM) technology, which in combination with new HapsTrak 3 I/O connectors delivers up to 3x prototype performance improvement over traditional connector and pin multiplexing technology. The new prototyping systems take advantage of a scalable architecture and the latest generation Xilinx Virtex-7 FPGA devices to support a wide range of design sizes with capacities from 12 to 144 million ASIC gates. The flexibility and matched pin connections between the Virtex-7's I/O banks and HapsTrak 3 connectors enable HAPS users to utilize I/O bandwidth where it is needed most while minimizing the number of unused pins.

"The stacked silicon interconnect technology of the Virtex-7 2000T FPGA delivers two million logic cells of capacity and 12.5 Gb/s serial transceivers, making it ideal for ASIC prototypes which require both high capacity and high-speed I/O," said Tim Erjavec, vice president of FPGA platform marketing at Xilinx. "The Synopsys HAPS-70 Series takes advantage of the Virtex-7 2000T FPGA's increased design capacity and I/O bank organization to deliver a system that eases design planning within and across multiple FPGAs while allowing the HAPS-70 to scale up to support multi-million gate ASIC SoC designs."

HAPS-70 systems are integrated with an intelligent prototyping software environment that enables faster partitioning and automates the creation and debug of prototypes for a range of designs from individual IP blocks and processor sub-systems to complete SoCs, easing the path from RTL to operational prototype. The modular architecture of the HAPS-70 systems enables engineers to use a common prototyping environment for IP and SoC software development, hardware/software integration and system validation, reducing duplication of effort across projects. New "HAPS-aware" features of Synopsys' Certify multi-FPGA prototyping software increase prototyping productivity by up to 10x with patent-pending algorithms to automate logic partitioning and live hardware queries to ease system bring-up compared to manual partitioning methods. The new prototyping systems also support HAPS Deep Trace Debug for greater debugging efficiency, providing approximately 100 times more signal storage capacity than the traditional memory storage employed by on-chip FPGA logic debuggers.

For easier system validation and software development, DesignWare Interface IP such as USB 3.0, PCI Express® and HDMI are validated on HAPS systems. With pre-validated DesignWare IP on HAPS systems and a rich selection of daughter cards for common IP protocols, designers can start software development earlier in the product development cycle and reduce IP integration effort.

"Synopsys' HAPS FPGA-based prototyping has been invaluable to Mindspeed for accelerating our hardware/software validation and improving our prototyping productivity," said Surinder Dhaliwal, executive director, VLSI Core Engineering, at Mindspeed Technologies, Inc. "As we continue to develop infrastructure product solutions, we are pleased that Synopsys has enhanced its FPGA-based prototyping family with higher performance, greater capacity and improved debug visibility targeted at larger, more complex designs like ours."

Synopsys' Universal Multi-Resource Bus (UMRBus) host connectivity option for the HAPS-70 system has been enhanced to support up to 400 MB/s bandwidth. The UMRBus provides a seamless link between HAPS-70 systems and Synopsys' Virtualizer-based virtual prototypes to create an integrated hybrid prototyping environment for early software development and hardware/software integration. The UMRBus also provides remote access, a generic C++/TCL programming interface and co-simulation with Synopsys' VCS® functional verification solution along with hierarchical block level bring-up and debug, enabling the HAPS-70 system to be incorporated into the design flow earlier.

"Increasing design size, software complexity and the earliest possible software development are key challenges for SoC prototypers," said John Koeter, vice president of marketing for IP and systems at Synopsys. "The extended capabilities of the HAPS-70 system further shorten software development and hardware/software integration by delivering industry leading FPGA-based prototyping capacity and performance with intelligent partitioning and debugging tools. By leveraging our technology leadership spanning hardware, software and IP, designers are immediately productive with validating their largest chip designs."

Availability & Resources
The HAPS-70 FPGA-based prototyping systems are available now to early adopters in nine model variants, with capacities from 12 to 144 million ASIC gates: HAPS-70 S12, HAPS-70 S24, HAPS-70 S36, HAPS-70 S48, HAPS-70 S60, HAPS-70 S72, HAPS-70 S96, HAPS-70 S120 and HAPS-70 S144, where S denotes ASIC Gate count supported.

- Hybrid Prototyping: https://www.synopsys.com/verification/prototyping/hybrid-prototyping.html
- HAPS Debug: https://www.synopsys.com/verification/prototyping/haps/haps-deep-trace-debug.html
- FPGA-based Prototyping Methodology Manual: https://www.synopsys.com/company/resources/synopsys-press/fpga-based-prototyping-methodology-manual.html
- FPGA-based Prototyping blog: http://blogs.synopsys.com/breakingthethreelaws/

HAPS-70 FPGA-based Prototyping at Embedded Technology / Electronic Design Solution Fair 2012:
Synopsys will be demonstrating the latest FPGA-based prototyping solution running on HAPS-70 hardware at Embedded Technology / Electronic Design Solution Fair, booth# D-35. The ET / EDS Fair takes place in Yokohama, Japan, November 14 –16, 2012. For more information on Synopsys' participation at ET / EDS Fair 2012 visit http://www.jasa.or.jp/et/ET2012/english/index.html

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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