Synopsys Announces DesignWare DDR4 Memory Interface IP

Memory Controller and PHY Support Multiple DDR Standards While Reducing Latency and Standby Power

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Highlights:

- Synopsys expands its industry-leading DesignWare® DDR Memory Interface IP family to include support for DDR4 SDRAMs
- Backward compatibility with DDR3 and LPDDR2/3 mobile SDRAMs gives SoC designers flexibility as they transition from one SDRAM standard to the next
- New DDR4 IP offers more features with up to 50 percent lower latency than the previous generation
- DDR4 memory controller and PHY are connected by a standard DFI 3.1 interface to streamline connections to custom PHYs and controllers

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced the expansion of its DesignWare DDR interface IP portfolio to include support for next-generation SDRAMs based on the emerging DDR4 standard. By supporting DDR4 as well as DDR3 and LPDDR2/3 in a single core, the DesignWare DDR solution enables designers to interface with either high-performance or low-power SDRAMs in the same system-on-chip (SoC), which is a key requirement of many SoCs such as applications processors for smartphones and tablets.

"Synopsys' support for DDR4 memory is an important contribution to building a robust DDR4 ecosystem," said Robert Feurle, vice president of DRAM marketing for Micron Technology, Inc. "DDR4 brings substantial power and performance benefits to the industry, and Micron is aggressively driving its introduction. By implementing their DesignWare DDR Interface IP with backward compatibility in mind, Synopsys is enabling chip developers to bridge the transition from today's DDR3-based SoCs to the upcoming DDR4 designs."

Synopsys' DesignWare DDR4 IP solution consists of the DDR4 multiPHY and Enhanced Universal DDR Memory Controller (uMCTL2) that connect through a commonly used DFI 3.1 interface. The new DDR4 IP supports all key DDR4 features planned for the upcoming JEDEC standard and, compared to the previous version, includes a 13 percent increase in raw bandwidth, up to a 50 percent reduction in overall latency and new low-power features that provide intelligent system monitoring and control to power down elements of the IP as determined by the system's traffic patterns. Real-time scheduling features in Synopsys' unique CAM-based DDR controller can optimize the scheduling of data read/write traffic from multiple hosts, maximizing performance and minimizing latency.

"While the initial target markets for DDR4 are networking, server, and compute platforms, engineers designing for digital TVs, set-top-boxes, multi-function printing, smartphone and tablet applications will also adopt DDR4 DRAM as prices drop and performance improves," said Desi Rhoden, executive vice president, Montage Technology, and JEDEC memory chairman. "Synopsys has leveraged their participation at JEDEC to develop DDR4-compatible products before the actual standard has been released, which is a key benefit of JEDEC membership."

"Synopsys' complete DDR interface IP portfolio includes support for LPDDR, LPDDR2, LPDDR3, DDR, DDR2, and DDR3," said John Koeter, vice president of marketing for IP and systems at Synopsys. "With this announcement, we are broadening our portfolio to include support for DDR4 while maintaining backward compatibility with existing JEDEC standard SDRAMs. As new DDR standards evolve, designers look for reliable solutions. Synopsys' track record of over 320 DDR IP design wins demonstrates that we offer a low-risk path to silicon success."

Availability

Availability for the DesignWare DDR4 multiPHY and Enhanced Universal DDR Memory Controller (uMCTL2) with support for DDR4 is planned for Q4 2012.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for system-on-chip (SoC) designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based

Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability of Synopsys' DesignWare DDR4 multiPHY and Enhanced Universal DDR Memory Controller (uMCTL2) with support for DDR4. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2012.

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