Latest Release of Synopsys IC Compiler Enables Giga-Performance Design

Continued Performance Focus Fortifies Widespread Deployment at Renesas Electronics

MOUNTAIN VIEW, Calif., July 18, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced the availability of the 2012.06 release of its IC Compiler™ software, featuring multiple advances to support giga-performance design. A key component of Synopsys' Galaxy™ Implementation Platform, IC Compiler has been addressing the productivity and manufacturability challenges inherent in giga-performance design through smarter optimization, faster design convergence and advanced process node support. This latest release of IC Compiler focuses on helping IC designers achieve higher clock frequencies more efficiently. New capabilities include innovative optimizations that can boost operating clock speeds, expanded support for highly fragmented floorplans and new technologies that address advanced process effects.

"Renesas Electronics is a premier provider of advanced semiconductor solutions," said Tatsuji Kagatani, department manager, Back-end Design Technology Development Department at Renesas Electronics Corporation. "We rely on continuous technology innovation in IC Compiler to realize our very challenging designs with clock speed targets of well over 1 GHz and/or lower power consumption with aggressive time to market goals. In our recent study of IC Compiler's new multisource CTS technology on a design with several complex clocks, we were easily able to meet our demanding skew and latency targets."

The IC Compiler 2012.06 release contains several new technologies geared towards boosting design frequency. Clock distribution using a mesh structure has been a staple of high performance designs to minimize variation. However, mesh flows are complex and require expert user knowledge to manage power efficiently. Multisource clock tree synthesis (CTS) is an innovative new technology that leverages automated clock tree and mesh techniques to provide better variation tolerance than traditional CTS, while consuming less power than a mesh.

Processor designers favor the performance scalability and smaller device geometries offered at lower process nodes. In this release, new algorithms leverage advanced process effects to improve timing, reduce buffer count and create more robust circuits for reduced variability. With shorter time-to-market windows and the need for a more integrated feature set, designs are seeing increasing intellectual property (IP) reuse. IP-dominated designs often have highly fragmented floorplans characterized by narrow channels between blocks and a large number of macros and pipelined registers. The latest IC Compiler release can improve timing and routability for such designs. The 2012.06 release also delivers several enhancements which enable designers to achieve target frequency. Transparent interface optimization technology has been improved to provide better timing and faster time to results. In-Design physical verification enables power network verification and improved runtime for foundry-required metal fill insertion.

"Renesas is a dominant presence in microcontrollers and embedded SoC designs," said Michael Jackson, vice president R&D, physical implementation, Synopsys. "We have worked closely with Renesas in delivering technology enhancements to boost performance and achieve faster design closure. The results of this successful collaboration can be seen by the continued leadership of IC Compiler in the physical implementation space."

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/**.**

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin

MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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