Synopsys and Samsung Deliver a Complete Solution for 20-Nanometer Node

Solution Includes Place and Route, Physical Verification, and Signoff Design Tools

MOUNTAIN VIEW, Calif., June 4, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq:SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems today announced the availability of a complete solution to enable engineers to develop state-of-the-art System-on-Chip (SoC) designs at Samsung's advanced 20-nanometer (nm) process geometry. The delivery of the solution is built on many years of close collaboration between Samsung Electronics and Synopsys R&D teams, including the tapeout of the first 20-nm chip based on Samsung's High-k metal gate process technology. The double-patterning enabled solution includes Synopsys' IC Compiler™ place and route solution, IC Validator physical verification product, StarRC™ extraction tool, and PrimeTime® timing signoff tool and all the required technology files, runsets, and rundecks. The combination of Samsung's 20nm process technology and the qualified Synopsys® tools from the Galaxy™ Implementation Platform enable predictable development of faster designs that use less area and less power.

"20 nanometer will be a very important process node which could change the landscape of the semiconductor industry," said Dr. Kyu-Myung Choi, senior vice president of System LSI infrastructure design center, Device Solutions, Samsung Electronics. "Our 20 nanometer collaboration with Synopsys, starting with our first 20 nanometer test chip tapeout, has allowed us to bring the best of 20 nanometer process technology to our mutual customers. In addition, our product teams are currently developing several next-generation SoCs for our 20 nanometer node that rely on Synopsys' Galaxy Implementation Platform."

"Broad deployment of the Galaxy Implementation Platform at Samsung for 20nm designs is the result of the strategic collaboration between the two companies," said Dr. Antun Domic, senior vice president and general manager of Implementation Group, Synopsys, Inc. "We have worked closely to address the new challenges introduced by 20nm node including double patterning technology. The collaborative innovations between Samsung and Synopsys will enable designers to manage power, performance, area, and time-to-market constraints by taking advantage of 20nm process technology to bring their best products to market."

20nm-ready Galaxy Implementation Platform

Samsung's qualification of Synopsys' Galaxy Implementation Platform is based on the two companies' R&D collaboration which developed comprehensive support for double-patterning technology and the hundreds of new rules related to finer geometries starting at 20nm. The Synopsys tools in the qualified flow include:

IC Compiler: Double-patterning aware placement, extraction and routing can deliver an optimal, DPT-compliant layout while minimizing any impact on area and performance

IC Validator: In-Design technology for fast detection and automatic repair of signoff-level DPT decomposition violations and yield detractor patterns, accelerating design closure for manufacturing compliance

PrimeTime: Added support for new multi-valued SPEF with minimal impact on runtime maintains signoff timing results at 20nm, including effects of double-patterning

StarRC: Silicon-calibrated modeling of parasitic variation addresses the effects of double patterning technology due to mask misalignment to enable accurate and high performance design

Details of Synopsys' 20-nanometer solution can be found at www.synopsys.com/20nm

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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