GLOBALFOUNDRIES Selects Synopsys' Yield Explorer for Faster Yield Ramp

Unique Fabless-Foundry Sharing Model Allows Automated Volume Diagnostics to Identify and Prioritize Systematic Failure Mechanisms

MOUNTAIN VIEW, Calif., May 30, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that GLOBALFOUNDRIES has selected Synopsys' Yield Explorer® solution as part of their next-phase Yield Management System (YMS) for faster yield ramp based on volume diagnostics. Rapid identification and correction of systematic failure mechanisms is critical to bringing a new technology node to production and driving the yield ramp on new integrated circuit (IC) designs. Yield Explorer Automated Volume Diagnostics allows GLOBALFOUNDRIES to quickly identify the dominant systematic failure mechanisms on early test chips as well as customers' chips, thereby reducing the time to achieve desirable yield levels. In addition, Yield Explorer's unique ability to combine and analyze data from design, fab and test domains enables collaboration between GLOBALFOUNDRIES and its customers to rapidly identify failure mechanisms and activate process or design corrective actions with high clarity and ease.

"Understanding and preventing the yield loss caused by design-process interactions is critical to ramp-up of designs manufactured on a new node," said Robert Madge, director of design enabled manufacturing at GLOBALFOUNDRIES. "Yield Explorer is a valuable new addition to our advanced Yield Management capabilities. Yield Explorer's unique data-sharing model very effectively addresses the sensitivity of design data, allowing strong collaboration with our customers during the yield ramp phase."

Yield Explorer delivers unparalleled flexibility and depth of capabilities in correlating yield loss to various design, fab and test attributes, as well as fast, robust automation for production analysis and reporting. Expert users benefit from the flexibility to perform analysis with an exploratory approach. Production teams rely on automated analysis routines to create various reports and provide a quick first view of yield issues on new production batches with minimal impact on cycle time. Additionally, any inputs to design teams for adjusting test plans or incremental layout changes are provided with specific and actionable details about the yield-limiting attribute of test or layout. The automated volume diagnostics in Yield Explorer are simple to deploy and work smoothly across a variety of design, fab and test outputs and data formats.

"Meeting yield targets for complex designs implemented on 28-nm and below technology requires understanding the complex interactions of design, lithography and process," said Howard Ko, senior vice president and general manager, Synopsys Silicon Engineering Group. "We are excited that GLOBALFOUNDRIES has chosen Yield Explorer to help them more quickly ramp-up new nodes and new designs."

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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