

# Samsung Electronics Tapes out Gigahertz+ ARM Cortex-A15 Processor with Synopsys IC Compiler

Hardened core used in industry's first ARM® Cortex™-A15 processor-based SoC for mobile computing devices

MOUNTAIN VIEW, Calif., April 30, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced the successful collaboration between Synopsys and Samsung Electronics on the implementation of an ARM Cortex-A15 MPCore™ processor. The processor core was implemented by Samsung Austin Research Center (SARC) using Synopsys IC Compiler place-and-route technology, a cornerstone of the Synopsys Galaxy™ Implementation Platform. Running at operating speeds in excess of a gigahertz on Samsung's 32nm low power process, the hardened core has already been deployed in the industry's first Cortex-A15 processor-based SoC for mobile computing devices. The high speed was enabled through a unique combination of innovative optimization techniques and differentiated high-performance technologies which have made IC Compiler the tool of choice for high-performance designs across multiple process nodes.

"Our mission is to deliver the highest frequency while minimizing power for high-end processor and graphics cores targeted to the mobile computing and digital home markets," said Keith Hawkins, vice president, SARC. "Globally, this was the first production tapeout of a Cortex-A15 processor and we relied exclusively on IC Compiler and the Galaxy tool suite to predictably achieve our performance and power targets."

Samsung fabricated the three-million-instance, dual-core Cortex-A15 processor on a 32LP high-K metal gate (HKMG) process. Synopsys collaborated closely with SARC on an implementation methodology based on key high performance technologies and optimization techniques in the Galaxy Implementation Platform to meet Samsung's stringent mass production criteria for an on-time tapeout. The processor core relied on Physical Datapath in Design Compiler® Topographical and IC Compiler for the structured placement of registers to meet power and area objectives. Layout-based debug with Design Compiler Topographical allowed quick analysis of library, netlist and placement issues to close timing. Clock mesh in IC Compiler and PrimeTime® provided the low skew and increased on-chip-variation (OCV) tolerance necessary for the high-performance core.

"Samsung is a leading provider of silicon in the mobile computing market, as can be seen by its smart phone and tablet market penetration," said Antun Domic, senior vice president and general manager, Implementation Group at Synopsys. "Being at the forefront of next generation mobile products, Samsung has driven many of the technology innovations that have reinforced the position of IC Compiler as the leading choice for high-performance design. The benefits of our ongoing partnership can be seen in the impressive level of performance delivered by this gigahertz-plus processor core."

## About Synopsys®

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

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