Latest Synplify FPGA Synthesis Software Offers New High-Reliability Features and Improves Productivity for FPGA-Based Prototyping

Synopsys' Synplify FPGA synthesis tools reduce runtime by up to 30 percent and add new soft error mitigation capabilities

Highlights:

- Continue-on-error capability that can significantly reduce the number of iterations required for design bring-up

- Triple Modular Redundancy and inference of error-correcting code RAMs reduces the effects of soft errors such as single-event upsets

- Fault-tolerant, finite-state machine implementation with Hamming-3 encoding delivers more reliable design operation

- Improved synthesis algorithms enable faster runtime

MOUNTAIN VIEW, Calif., April 2, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq:SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced availability of the latest release of its Synplify Pro® and Synplify® Premier FPGA synthesis tools. The Synplify 2012.03 products include improved synthesis algorithms that accelerate runtime by up to 30 percent. In addition, the Synplify Premier software is enhanced with a new continue-on-error feature to address FPGA designers' need for fast turnaround time by enabling them to generate a report and fix all errors resulting from missing or incorrect design definitions at the end of the hardware description language (HDL) compilation step rather than incrementally fixing an error and rerunning the compile step. This capability is especially important with SoC prototypers who may not be intimately familiar with the HDL code they have to implement in an FPGA. Additionally, the new Synplify Premier software release further automates the process of building high reliability and fault tolerance into an FPGA design using a combination of advanced features including selective triple modular redundancy (TMR), fault-tolerant error correcting code (ECC) memories and Hamming-3 encoding for detection and correction of soft errors.

"Our customers continue to face shorter time-to-market windows, making it essential they complete their designs faster," said Alex Grbic, director of marketing for software, DSP and IP at Altera. "The runtime improvement in Synopsys' Synplify products combined with the compile time advantage we have in our Quartus II software provide our mutual customers a productivity edge that allows them to reduce overall implementation time when designing for our latest 28-nm FPGAs."

"Designs targeted for safety critical applications such as those used in defense, aerospace, medical, industrial control and automotive markets require the highest level of quality and reliability," said Tom Feist, Senior Director of Design Methodology Marketing at Xilinx. "The new 2012.03 Synplify Premier product infers Xilinx error correcting memory and automatically makes the connections to the design. This is especially useful for high reliability applications where errors cannot be tolerated."

The new Synplify 2012.03 software release offers FPGA designers significantly shorter design cycles. The continue-on-error feature addresses FPGA-based prototypers' need for fast turnaround time by eliminating the need to address errors one at a time as they are found during HDL compilation. It is especially useful for FPGA-based prototypers who may not be as familiar with the source HDL code. Instead of stopping with each error, the tool continues compilation after an error is found, generating a report of all the errors encountered so that they can be addressed at once, without re-compiling between each fix. To further simplify the process for ASIC prototypers, the Synplify synthesis tool has a datapath latch conversion feature to automatically convert an ASIC design to an FPGA implementation, making it possible for the designer to use a single set of source files to implement the FPGA-based prototype. Users of Synopsys' Certify® multi-FPGA prototyping environment also benefit from the streamlined error-handling and conversion features in the new Synplify software, which helps speed the validation process and reduce development time.

The latest release of the Synplify Premier software enhances its support for high reliability by giving designers the ability to address radiation effects such as single event upsets (SEUs) through multiple error mitigation techniques including localized and selective TMR implementation. In addition, the Synplify Premier software can infer error correcting memory and automatically make the proper connections to take advantage of ECC memories offered by FPGA vendors. The latest release also supports fault-tolerant finite-state machine (FSM) implementation using Hamming-3 encoding to automatically detect and correct single bit errors that might

occur in the registers of an FSM.

"Rapid bring-up of a new design is critical for design teams trying to meet tight market windows. And Synopsys synthesis technology can reduce the number of design iterations and provide diagnostic information sooner," said Ed Bard, senior director of marketing of the Solutions Group at Synopsys. "With the combination of improved algorithms that deliver faster runtimes and the new continue-on-error feature and hierarchical design techniques, FPGA-based prototypers and FPGA designers alike can significantly reduce the time required to get a working implementation of their design while continuing to see the high quality of results they expect from Synplify tools."

Availability
The 2012.03 release of the Synplify Pro and Synplify Premier synthesis software is available now. Customers with a current maintenance agreement can download this new version from Synopsys using their SolvNet® account. The Synplify FPGA synthesis products are supported on Windows and Linux, 32 and 64-bit platforms.

About Synopsys®
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.