Synopsys' Collaboration with Industry Consortium Yields Double Patterning Technology Models for Parasitic Extraction

IMTAB Group in IEEE-ISTO Ratifies Interconnect Technology Format Extensions for 20nm

MOUNTAIN VIEW, Calif., March 28, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that its collaboration with the members of the Interconnect Modeling Technical Advisory Board (IMTAB) of the IEEE Industry Standards and Technology Organization (IEEE-ISTO) has resulted in a parasitic variation modeling solution to address the effects of double patterning technology (DPT), targeted for use in 20-nanometer (nm) IC manufacturing. The new DPT model extensions will be available to the EDA and semiconductor industries through the open source licensed Interconnect Technology Format (ITF) version 2012.06 ratified by IMTAB members, including Apache Design – a subsidiary of ANSYS, GLOBALFOUNDRIES, NVIDIA, Synopsys and others (the full member list is available at www.imtab.org).

DPT is a critical technique for ensuring printability of device and interconnect layers in 20-nm IC manufacturing. However, splitting layers into two masks can introduce timing variations as a consequence of mask misalignment in the manufacturing process. To enable successful 20-nm design tapeouts and manufacturing, the IMTAB members determined that a DPT-aware modeling solution for parasitic extraction was needed to account for the timing impact and address it in the physical implementation and signoff design flow.

"The real challenge was developing a solution that accurately modeled the impact on timing with no productivity change to the flow," said Bari Biswas, chair of IMTAB and senior director of engineering for extraction solutions at Synopsys. "While working with IMTAB and leading foundries, Synopsys developed a novel modeling technique that eliminates the need to insert the time-consuming coloring step during the implementation and signoff flow, with negligible impact on extraction runtime."

"The manufacturing requirements at advanced process nodes, such as double-patterning lithography at 20-nanometers, are driving an industry-wide, intensive focus on newer parasitic modeling techniques to achieve signoff accuracy and performance," said Richard Trihy, director of design methodology at GLOBALFOUNDRIES. "GLOBALFOUNDRIES is pleased to be working with the industry-leading IMTAB member companies and lending our extensive knowledge of advanced processes to develop innovative solutions that address these common challenges. Our close collaboration has resulted in several enhancements to ITF modeling at the 28-nanometer node, and GLOBALFOUNDRIES is now driving silicon-validation of the latest DPT modeling at the 20-nanometer node."

In addition to DPT modeling, IMTAB has also approved enhanced trench contact device modeling extensions in the ITF to include evolving 20-nm characteristics. The trench contacts are used for local device interconnections that improve density and lower resistance. However, additional challenges are introduced in modeling co-vertical conductors and associated large fringe capacitances. To deal with these issues, specific 20-nm extensions were added to explicitly model silicon dielectric underneath the device and the special dielectric region between the gate and raised diffusion to enable accurate modeling of the new parasitic effects.

"IMTAB members continue to collaborate on challenges facing the semiconductor industry in new process nodes such as 20-nanometer," said Marco Migliaro, president and CEO at IEEE-ISTO. "To improve tool interoperability around ITF modeling, IMTAB will help the industry realize a single, proven format to help speed design flows."

The next IMTAB meeting is scheduled for Tuesday, May 22, 2012. The confirmation of the date and agenda, focusing on 20nm modeling, will be posted on the IEEE-ISTO's IMTAB website: www.imtab.org.

Requests for ITF format enhancements come from the IMTAB membership as well as from the overall interconnect modeling format user community. Companies interested in IMTAB membership may contact IEEE-ISTO at imtab@ieee-isto.org.

About ITF

Synopsys' Interconnect Technology Format (ITF) provides detailed modeling of interconnect parasitic effects that enables designers to perform accurate parasitic extraction for timing, signal integrity, power and reliability signoff analysis. ITF offers a flexible and innovative format to accurately model the effects of increased process variation at advanced process technologies. Proven on thousands of production designs, ITF has been evolving for more than 10 years and is the semiconductor industry's most widely used interconnect modeling format. It is supported by leading semiconductor foundries, integrated device manufacturers and EDA tool providers.

The ITF format can be licensed for no charge through Synopsys' Technology Access Program (TAP-in(SM)). The latest specifications for ITF can be found at: www.synopsys.com/TapIn.

About IEEE-ISTO

IEEE-ISTO is the premier trusted partner of the global technology community for the development, adoption and certification of industry standards. Its mission is to facilitate the life-cycle of industry standards development through a dedicated staff committed to offering vendor neutrality, quality support and member satisfaction. Fostering the market acceptance, adoption and implementation of standardized technologies, IEEE-ISTO programs span the spectrum of today's information and communications technologies. To find out more about IEEE-ISTO, visit www.ieee-isto.org.

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Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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