Synopsys Introduces Industry's First 28-nm Multi-Gear MIPI Alliance M-PHY IP Supporting Six Standards for Mobile Applications

Scalable DesignWare MIPI M-PHY IP future-proofs mobile SoC designs while providing low power, low latency and compact footprint

BARCELONA, Spain, Feb. 29, 2012 /PRNewswire/ -- MOBILE WORLD CONGRESS -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced availability of a new DesignWare® MIPI M-PHY IP solution supporting multiple speed gears and a broad range of high-speed interfaces for mobile applications. Based on the industry's first silicon-proven DesignWare MIPI M-PHY IP introduced by Synopsys in 2010, the new MIPI M-PHY IP is the first 28-nanometer (nm) multi-gear solution that supports six different inter-chip interconnect protocols including the JEDEC Universal Flash Storage (UFS), the USB SuperSpeed Inter-Chip (SSIC), and the MIPI Alliance's Low Latency Interface (LLI), DigRF v4 and future CSI-3 and DSI-2 interfaces. By providing application-oriented M-PHY IP that runs at multiple speeds and is interoperable with multiple protocols, Synopsys enables design teams to "future-proof" their designs while reducing the risk and cost of integrating MIPI interfaces into basebands, application processors and mobile ICs.

The 28-nm DesignWare MIPI M-PHY IP offers Type-I and Type-II low-speed implementations to support different application requirements. With support for high-speed GEAR1, GEAR2 and GEAR3, ranging from 1.248Gbps to 5.8Gbps, this scalable solution can meet ever-increasing data rate requirements, enabling reuse of proven IP in next-generation devices. Using a variety of high-speed and low-speed burst modes and power management modes, including idle, sleep and hibernate with quick entry and exit capability, Synopsys' DesignWare MIPI M-PHY IP can be optimized to achieve required data rates while meeting the stringent power and area requirements of mobile SoCs.

"Synopsys is regarded as a technology leader in the development of MIPI IP, and we are continuing our successful collaboration to deliver the future-proof DesignWare MIPI M-PHY IP with the Tektronix M-PHY test suite," said Mike Rizzo, technology solutions manager at Tektronix. "Our M-PHY test suite includes the popular DSA70000 Series Oscilloscope and allows M-PHY users to test the M-PHY electrical functionality and integrate high-speed MIPI interfaces into mobile chipsets."

"As a longtime contributor to the MIPI working groups, Synopsys continues to help drive MIPI specifications to build a robust mobile ecosystem," said Joel Huloux, president and chairman, MIPI Alliance. "The new DesignWare MIPI M-PHY IP will likely prove useful to designers and expand their interface choices."

The DesignWare MIPI M-PHY IP is compliant with the MIPI Alliance M-PHY v1.0 specification. By working closely with the MIPI Alliance to develop its specifications, Synopsys targets its IP to comply with future MIPI M-PHY specification releases. Synopsys DesignWare MIPI M-PHY IP supports High Speed GEAR1, GEAR2 and GEAR3 rates A/B along with Type-I and Type-II low-speed capabilities. The DesignWare MIPI M-PHY's modular architecture allows implementation of a variety of transmitter and receiver lanes to meet a broad range of system requirements and all modes outlined in the protocol specification. A sophisticated clock recovery mechanism and power efficient clock circuitry are designed to maintain the integrity of the clocks and signals required to meet strict timing requirements. The DesignWare MIPI M-PHY supports large and small amplitudes, slew rate control and dithering functionality for optimized electromagnetic interference (EMI) performance.

"With an increasing number of devices integrating mobile functionality, IP solutions supporting mobile standards must be capable of meeting the power and performance targets of multiple end applications," said John Koeter, vice president of marketing for IP and systems at Synopsys. "With support for multiple speed gears and interface protocols, the 28-nanometer DesignWare MIPI M-PHY gives designers a high-quality IP solution that can reduce the risk of integrating MIPI interfaces into their SoCs today with the scalability needed to address faster data rates in the future."

Availability
The multi-gear DesignWare MIPI M-PHY IP in the 28-nm process node will be available for early adopters in calendar Q2, 2012. For more information, visit: http://www.synopsys.com/mipi.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. To support software development and hardware/software integration of the IP, Synopsys offers drivers,

transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to following traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys®
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

Forward Looking Statements
This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability of DesignWare MIPI M-PHY IP on 28-nm process node. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2011.

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