Synopsys Enables Silicon Success for GLOBALFOUNDRIES' First Complex 20-nm Design

GLOBALFOUNDRIES Tapeout Reinforces Synopsys IC Compiler as the Leading Choice for 20 Nanometers

MOUNTAIN VIEW, Calif., Dec. 14, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that IC Compiler-Advanced Geometry (AG) drove silicon success for GLOBALFOUNDRIES' first major 20-nanometer (nm) chip. Recently announced, IC Compiler-AG is the 20-nm edition of IC Compiler. The tapeout of this large design containing a dual-core processor represents a major milestone in the collaboration between Synopsys and GLOBALFOUNDRIES to develop 20-nm rules and a comprehensive double patterning technology (DPT)-aware implementation solution. The selection of IC Compiler for this critical design further strengthens IC Compiler's technological leadership in 20-nm design. Other components of Synopsys' Galaxy™ Implementation Platform were also used in the design, including StarRC™ extraction and PrimeTime® static timing analysis.

"We relied exclusively on IC Compiler-AG for the implementation of this complex 20- nanometer dual-core processor design," said Mojy Chian, senior vice president of design enablement at GLOBALFOUNDRIES. "Furthermore, we extensively used IC Compiler Zroute technology for the necessary rule formulation to ensure manufacturability compliance. Our close collaboration with Synopsys resulted in robust implementation of DRC and double patterning rules and enabled us to get to tapeout in time and with high manufacturing fidelity."

At 20nm, as with prior process-node transitions, the challenges of managing power, performance, capacity and variability become progressively complicated. But, 20nm also introduces a clear, new challenge—double patterning technology (DPT). This places an unprecedented burden on place and route tools to efficiently generate a layout which not only meets the traditional metrics mentioned above, but also can be decomposed into dual alternating patterns without undue impact on performance or device area.

Typical solutions for DPT either force full complexity of DPT in the place and route tool, incurring potentially large runtime and die-size overhead, or rely on an implement-then-verify approach to verify DPT correctness with a physical verification tool, risking multiple schedule-destroying iterations. Synopsys' IC Compiler-Advanced Geometry is built on award-winning Zroute and IC Validator In-Design physical verification technologies to deliver a noticeably superior DPT solution that minimizes die size and timing overhead while enabling the fastest path to design closure. Synopsys' approach to DPT keeps place and route performance efficient and avoids late-stage surprises, speeding the final tapeout. IC Compiler's DPT enhanced placement engine and Zroute routing technology work in tandem to efficiently generate a DPT-aware layout that can be verified and repaired for residual DPT violations using In-Design physical verification with IC Validator. GLOBALFOUNDRIES is actively partnering with Synopsys to offer this flow concurrently with the commercial release of its 20-nm technology.

"GLOBALFOUNDRIES is a market leader at the forefront of innovative technology development and we have a standing commitment to work together which has resulted in this successful tapeout," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "This tapeout adds to the growing list of successful 20-nm designs that have been completed using IC Compiler-AG, further underscoring its technological leadership. We will continue to collaborate with GLOBALFOUNDRIES to address the additional complex requirements of 20-nm design by providing the best quality implementation environment."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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