Synopsys' IC Validator Certified by GLOBALFOUNDRIES for 28-nm, 40-nm and 65-nm Design

Runset Availability Brings Benefits of In-Design Physical Verification to Mutual Customers

MOUNTAIN VIEW, Calif., Dec. 8, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that GLOBALFOUNDRIES has certified Synopsys' IC Validator physical verification product for 28-nanometer (nm), 40-nm and 65-nm physical signoff, with immediate availability of design rule checks (DRC) and layout-versus-schematic (LVS) runsets to GLOBALFOUNDRIES customers. IC Validator, part of the Galaxy™ Implementation Platform, is an ideal add-on to IC Compiler for In-Design Physical Verification, making it possible for place and route engineers to accelerate time to tapeout by eliminating late-stage surprises and manual fixes. GLOBALFOUNDRIES' qualification of IC Validator brings the unique benefits of In-Design Physical Verification to design teams working with GLOBALFOUNDRIES' 28-nm, 40-nm and 65-nm process nodes.

"GLOBALFOUNDRIES is committed to making available to its customers solutions that ensure silicon success while optimizing design turnaround time. As such, optimal runset creation and efficient maintenance are paramount to our success," said Mojy Chian, senior vice president of design enablement at GLOBALFOUNDRIES. "Runset creation with IC Validator was completed in record time and led to full certification for our 28-, 40- and 65-nanometer process nodes. Our customers can now benefit from IC Compiler In-Design technology by using our sign-off quality runsets during design to avoid late-stage surprises and ensure a smooth hand-off to manufacturing."

In today's demanding design environment, the customary implement-then-verify approach has become a bottleneck, causing late-stage surprises and leading to an increase in time-consuming and error-prone design iterations. In-Design Physical Verification, based on intelligent integration of IC Validator and IC Compiler, enables place and route engineers to perform independent signoff-quality analysis earlier, before the design is finalized and while correction can be automated. In-Design technology enables new high-productivity functionality, such as automatic DRC repair, timing-aware metal fill and rapid ECO validation, all within the place and route environment. With In-Design Physical Verification, expensive iterations with downstream analysis tools are eliminated and convergent design evolution to physical signoff is maintained.

IC Validator utilizes its scalable hybrid data and command-processing engine to offer a powerful platform for coding and validating the complex polygon and edge-based rules required for emerging process nodes. It enables coding at higher levels of abstraction, automating tedious lower-level data processing. IC Validator is architected for near-linear scalability that maximizes utilization of mainstream hardware, using smart, memory-aware, load scheduling and balancing technologies. These capabilities will enable GLOBALFOUNDRIES to streamline design rule development and deployment and offer mutual customers the high accuracy and excellent scalability necessary for advanced process nodes.

"As manufacturing complexity places increased pressure on our customers to deliver within schedule, it is very important that we continue to collaborate closely with leading foundries like GLOBALFOUNDRIES," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "This certification brings the proven benefits of In-design Physical Verification, which have been replicated by a number of design teams worldwide, to GLOBALFOUNDRIES' customers working at advanced nodes with IC Compiler."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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