Synopsys Leads the Way in Delivering Dual-Patterning-Compliant 20nm IC Implementation Support

Builds on Award-Winning IC Compiler Zroute and IC Validator In-Design Physical Verification Technologies

MOUNTAIN VIEW, Calif., July 11, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced IC Compiler-Advanced Geometry, a new configuration of its market-leading IC Compiler physical design product. IC Compiler-Advanced Geometry targets design support for double-patterning technology (DPT), which has emerged as a key requirement for the next generation of silicon technology at 20 nanometers (nm) and imposes strict constraints on placement, routing and physical verification. As industry leaders in IC design and manufacturing race to prepare for 20nm technology, Synopsys has successfully collaborated with foundry partners as well as major customers to validate that IC Compiler is 20nm-ready. IC Compiler, a key component of the Galaxy™ Implementation Platform, provides one of the most efficient DPT-ready physical implementation solutions with minimal impact on turnaround time and traditional design metrics of device area, speed, and power.

The current lithography approach supporting IC manufacturing reaches a theoretical limit at the 20nm node, making it difficult to achieve minimum resolution for silicon structures. There are two possible approaches: 20nm design must either adopt a resolution that is sparser than minimum, and therefore not silicon-efficient; or the design must be split into two sets of alternating structures, each more sparse than minimum but together fully utilizing available silicon resource. The latter, termed double-pattern technology, requires a place-and-route tool to accurately generate a layout where each candidate layer can be decomposed into dual alternating patterns without undue impact on performance and device area.

The new configuration of IC Compiler includes innovative technology to formulate double patterning requirements as a generalized coloring problem, avoiding any potential conflicts and rendering a correct-by-construction solution that can be reliably decomposed during manufacturing. Central to this solution is IC Compiler's placement engine and the award-winning Zroute technology, which have both been enhanced to be DPT-driven. In addition, IC Validator's In-Design Physical Verification has been enhanced for DPT compliance, enabling IC designers to verify before handoff to manufacturing that target layers in the design are decomposable.

"Design and manufacturing complexity continues to rise, and designers are under increased pressure to adapt and deliver. As a result, it is imperative that we collaborate closely with our foundry partners and key customers to be the first to offer a compelling design implementation solution," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "IC Compiler-Advanced Geometry is the industry's first DPT-compliant place-and-route solution that will provide designers moving to 20 nanometers with an advanced solution that effectively meets the new challenges."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding Synopsys' anticipated ability to timely enable the design and validation of 20-nanometer process technology in the future. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, technical or other difficulties in enabling 20-nanometer solutions, design delays, specific customer configurations and other risks as identified in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of the latest Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2011.

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