Synopsys Delivers 28-nm Design Solutions and Advanced System-Level Capabilities for TSMC Reference Flow 12.0

Flow provides optimized methodologies to shorten time-to-market and time-to-volume for designers using TSMC's 28-nanometer process technology

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Highlights:

- Synopsys provides comprehensive support for TSMC's 28-nanometer (nm) technology for manufacturing compliance from physical design through to signoff.
- Synopsys' Virtual Prototyping, as a part of TSMC's silicon design flow, allows project teams to develop software and tune hardware architecture before silicon is available.
- Synopsys' software-driven verification using UVM methodology links to hybrid virtual prototypes for testbench reuse, results in faster verification.
- High-level synthesis from Synopsys is optimized for TSMC's advanced process technologies for performance- and power-optimized designs using C/C++ code.

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that it is delivering comprehensive design enablement for TSMC's 28-nm process technology, integrated manufacturing compliance and an advanced system-level prototyping solution, with TSMC Reference Flow 12.0. New features of the flow include virtual prototyping and high-level synthesis linked to TSMC's advanced processes, expanded manufacturing compliance capabilities and full support of TSMC's latest 28-nm design rules and models within Synopsys' Galaxy™ Implementation Platform. With the new tool capabilities and system-level design integration, designers gain productivity, shortened time-to-market and faster time-to-volume using TSMC's 28-nm process technology.

"TSMC and Synopsys collaborated on Reference Flow 12.0 to increase productivity and design quality with an optimized design methodology for our mutual customers," said Suk Lee, director of design infrastructure marketing at TSMC. "The combination of Synopsys tools, IP and system-level design and prototyping capabilities with TSMC's complete 28-nm design infrastructure and advanced process technology provides designers with a comprehensive solution that addresses manufacturability while enabling design for optimized performance."

Synopsys has extended Reference Flow 12.0 to deliver a consistent and comprehensive methodology for earlier development and faster verification of software stacks and hardware platforms using Synopsys' Virtual Prototyping and Synphony C Compiler high-level synthesis solutions. The virtual prototype authoring tool, combined with Synopsys' open transaction-level-modeling (TLM)-2.0 model library, enables designers to quickly and automatically generate and integrate models and interconnects to create virtual prototypes. The integration of TSMC's Power Performance Area model in the flow allows hardware and software designers to make TSMC technology node- and software-specific tradeoffs months earlier in the design flow. The system-level flow links SystemC™ TLM 2.0 and RTL models in Synopsys' VCS®- based verification solution using the UVM methodology and hybrid virtual prototypes, enabling verification environment reuse and software-driven verification. Synphony C Compiler high-level synthesis has been optimized for TSMC's advanced process technologies, allowing designers to quickly achieve performance- and power-optimized results using high-level C/C++ code.

The flow includes a comprehensive ARM® Cortex™-A9 MPCore™ Fast Model-based reference Virtual Prototype, which has been extended with a TSMC example H.264 video subsystem. In conjunction with the included Linux SMP kernel and file system, this example serves as a practical template for early hardware/software stack integration and demonstrates the full virtual prototyping debug and analysis capabilities. Fully documented reference design examples for Synphony C Compiler are also included in the flow.

The Synopsys Galaxy Implementation Platform features comprehensive support for TSMC's latest 28-nm design rules for manufacturing compliance from physical design through to signoff. Additionally, Reference Flow 12.0 includes IC Compiler's leakage optimization engine for final-stage leakage recovery on a close-to-tapeout design. Reference Flow 12.0 adds IC Validator's patented pattern-matching technology to extend the advantage of IC Compiler's In-Design physical verification by enabling fast detection and automated repair of manufacturing-limiting layout patterns.

"Designers are looking to make the most of TSMC's most advanced process nodes through a convergent and predictable path that helps them successfully develop a system-on-chip from system-level concept to silicon," said Rich Goldman, vice president of corporate marketing and strategic alliances at Synopsys. "Synopsys and TSMC team to deliver unique analysis, verification and implementation solutions in Reference Flow 12.0, offering our mutual customers an optimized path to achieve their aggressive system-on-chip design goals."

About Synopsys Support for TSMC Reference Flow 12.0

TSMC Reference Flow 12.0 comprises of a comprehensive set of Synopsys system-level, design implementation and verification tools, and IP including:

System-Level Design

- Virtual Prototyping and DesignWare® System-Level Library for SoC virtual prototyping and power/performance analysis
- Synphony C Compiler high-level synthesis feeding into DesignCompiler® Ultra

DesignWare IP

- DesignWare IP and Verification IP for the ARM AMBA® interconnect provides infrastructure and fabric components for AMBA 2.0 and AMBA 3 AXI3™
- Automated assembly of the IP using coreAssembler tool

Verification

- CustomSim™ and HSPICE® circuit simulation with TSMC 28-nm model support
- VCS with MVSIM voltage-aware simulation
- MVRC low power static checking
- SoC ESL verification using VCS with UVM 1.0

Physical Implementation

- IC Compiler place and route, including Zroute technology and dummy via insertion
- IC Validator DRC/LVS In-Design physical verification and sign-off

RTL Synthesis and Test

- DC Ultra™ and Design Compiler Graphical RTL synthesis including Topographical technology and congestion optimization
- DesignWare Library datapath IP
- Power Compiler™ power optimization and multi-voltage power management
- Formality® equivalence checking
- DFTMAX™ compression for test cost reduction
- TetraMAX® automatic test pattern generation (ATPG)

Analysis and Sign-off

- PrimeTime® static timing analysis including advanced stage-based OCV

- StarRC™ parasitic extraction with feature-scale VCMP, eDRAM tall contact, via-etch and trench contact modeling support
- PrimeYield LCC for automatic lithography-hotspot and pattern-match detection and fixing, and TSMC unified LPC format support
- Parasitic extraction, timing, IR-drop analysis

Rapid Yield Ramp

- Yield Explorer for physical pattern-aware, design-centric volume diagnosis isolates and prioritizes the dominant systematic failures among the scan diagnostics results
- Integration of systematic defect simulation data into yield analysis to quickly capture process marginality impacts on scan failures

Synopsys Professional Services is a global member of TSMC's Design Center Alliance, providing expertise in chip implementation and flow deployment with the Lynx Design System and Reference Flow 12.0. TSMC Nexsys Standard Cells and I/Os are available to DesignWare Library licensees at no additional cost.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/**.**

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