Synopsys Advances Mixed-Signal Verification with New CustomExplorer Ultra

Advanced Regression and Analysis Environment Streamlines Mixed-signal Verification and Boosts Productivity

Highlights:

- Regression automation
- Advanced analysis and debug
- Heterogeneous netlist support for SPICE, Verilog, Verilog-A, Verilog-AMS, SystemVerilog

MOUNTAIN VIEW, Calif., April 18, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the immediate availability of the CustomExplorer™ Ultra mixed-signal verification environment as part of Synopsys' Discovery™ Verification Platform. CustomExplorer Ultra provides a comprehensive regression and analysis environment to increase verification productivity and streamline the verification process for analog and mixed-signal designs. The combination of CustomExplorer Ultra and Synopsys' CustomSim™/VCS® mixed-signal verification solution provides design teams with a high-performance, productive mixed-signal simulation and regression management environment for complex system-on-chip (SoC) verification.

"With the increasing number of mixed-signal circuits in SoCs, verification teams are demanding a high-productivity environment to significantly reduce the complexity of mixed-signal verification tasks," said Paul Lo, senior vice president and general manager, Synopsys Analog/Mixed-Signal Group. "CustomExplorer Ultra complements our strong CustomSim/VCS mixed-signal verification solution to provide design teams with a scalable solution to tackle the verification challenges of complex mixed-signal SoCs."

Regression Automation

CustomExplorer Ultra is seamlessly integrated with the CustomSim/VCS mixed-signal verification solution. Multiple testbench and corner configurations can easily be set up, and simulation jobs are automatically queued and submitted to the server farm. Simulation job distribution and monitoring gives real-time status of multiple jobs running on multiple machines, providing quick feedback if problems are detected during simulation.

Advanced Analysis and Debug

Simulation results are collected, processed and presented in a spreadsheet-style display, providing an easy-to-read visual summary of the verification tests. Pass/fail results are indicated in the display, and the results can be filtered by design, design variables, equation results, or equation expressions. The unique Waveform Compare technology in CustomExplorer Ultra can be used to compare simulation results to a known-good waveform, saving considerable analysis time. The CustomExplorer Ultra debug environment offers complete SPICE linting, design hierarchy file browsing and signal tracing, as well as cross-probing between netlists, waveforms and interactively-generated connection visualization for rapid debugging. CustomExplorer Ultra is integrated with Custom WaveView (included), enabling waveform cross-probing and sophisticated waveform measurements. Together, these features aid designers in rapidly performing customized advanced analyses in a powerful design verification and debugging environment for analog and mixed-signal designs.

Heterogeneous Netlists Assembly

Netlists can be imported from a variety of heterogeneous sources and assembled into a single simulation netlist for verification using the configuration manager; SPICE, Verilog, Verilog-A, Verilog-AMS and SystemVerilog formats are supported. CustomExplorer Ultra's ability to assemble heterogeneous netlists from multiple sources greatly enhances the automation of mixed-signal verification.

Availability

The CustomExplorer Ultra mixed-signal verification environment is available immediately.

CustomExplorer Ultra Webinar

Synopsys will host a webinar entitled "Advanced Regression and Analysis for Mixed-Signal Verification Using CustomExplorer Ultra" premiering at 10:00 a.m. on Wednesday, May 11, 2011. This webinar will demonstrate how CustomExplorer Ultra enables high verification productivity for complex SoCs using advanced strategies that surpass traditional verification approaches. People interested in viewing this webinar can register online. All Synopsys webinars are listed on the web site at www.synopsys.com/Company/Pages/WebinarTopics.aspx.

Related Links

- CustomExplorer Ultra Data Sheet
- CustomExplorer Ultra Mini Demo
- CustomExplorer Ultra Technical Backgrounder
- CustomExplorer Webinar

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.