Synopsys Announces Availability of DesignWare PHY and Embedded Memory IP for TSMC Advanced 28-nanometer Technologies

Achieving USB Logo Certification for DesignWare USB 2.0 picoPHY Demonstrates Success of Collaboration

MOUNTAIN VIEW, Calif., March 30, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that it has worked with TSMC to develop a broad portfolio of DesignWare® interface PHY IP including SuperSpeed USB 3.0, USB 2.0, HDMI, PCI Express®, DDR and SATA as well as embedded memories for TSMC's 28-nanometer (nm) process technology. The collaboration enables designers to incorporate more functionality into their advanced system-on-chips (SoCs), while meeting low power and small silicon area requirements.

As a result of this collaboration, Synopsys has achieved USB logo certification for the DesignWare USB 2.0 picoPHY IP in TSMC's 28-nm process, demonstrating a robust design architecture that can withstand rigorous process, voltage and temperature variations. In addition, the DesignWare IP portfolio of SiWare® Embedded Memory SRAMs has also achieved positive silicon results for TSMC's 28-nm process. The longstanding cooperation between the two companies has resulted in the development of DesignWare PHY IP from 180-nm to 28-nm process technologies, allowing design teams to integrate key industry standard interfaces into their designs with less risk and improved time-to-market.

"TSMC's close relationship with Synopsys through the years has provided mutual customers access to a broad portfolio of high-quality IP solutions for a wide range of TSMC processes," said Suk Lee, director of Design Infrastructure Marketing Division, at TSMC. "Our collaboration with Synopsys on the development of DesignWare PHY and Embedded Memory IP for TSMC's advanced 28-nm process is a natural extension of our successful track record, and further demonstrates our shared commitment to delivering to designers widely-used SoC functionality for their high-performance, low power mobile designs."

"Synopsys' collaboration with TSMC has helped designers cope with the challenges of incorporating advanced interfaces into their SoCs," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "By providing a broad portfolio of IP that has been silicon-proven to be robust in process, voltage and temperature variations for TSMC processes, we can continue to help customers reduce integration risk and speed their creation of differentiated SoCs."

Availability

The DesignWare PHY IP for the TSMC 28-nm process is scheduled to be available in Q2 of 2011. The DesignWare IP portfolio of SiWare Embedded Memories for the TSMC 28-nm process is available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols, analog IP, embedded memories, logic libraries, embedded test & repair IP and configurable processor cores. In addition, Synopsys offers SystemC transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and date of availability of the DesignWare PHY IP for the TSMC 28-nm process. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2010 entitled "Risk Factors."

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