

Synopsys Announces New Technology for Optimizing Multicore Systems

Platform Architect Enables Early Architecture Definition, Hardware-Software Partitioning and Performance Analysis of Multicore Systems Months before Software is Available

Highlights:

- New Multicore Optimization Technology for Synopsys Platform Architect makes creating and utilizing performance models of dynamic multicore applications highly effective in SystemC.
- By capturing performance models of dynamic multicore applications in the early concept phase of system architecture design, architects can measure, analyze and optimize the hardware/software system architecture months before the software is available.
- Platform Architect with Multicore Optimization Technology reduces the risk of over-design and/or under-design in consumer, wireless communications and automotive system design, helping ensure cost-effective and successful products.

MOUNTAIN VIEW, Calif., Feb. 7, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the broad availability of Platform Architect with Multicore Optimization Technology, a new solution for performance analysis and early definition of multicore system architectures in SystemC. Using Platform Architect with Multicore Optimization Technology, designers of SoCs, chipsets and systems can capture hardware/software performance models of multicore system architectures in the early concept phase for robust performance measurement and trade-off analysis, months prior to software availability.

"Given the escalating costs of SoC design, system architects have a difficult task in defining the optimum system architecture to support all the desired application use-cases in a cost-effective way," says Rene van den Berg, system architect, car entertainment solutions, NXP Semiconductors. "The new Multicore Optimization Technology embedded in Synopsys' Platform Architect gives architects a clear understanding of the application and required features in an early stage of the project. With this insight on system performance, the hardware and software allocation of available resources, software scheduling scenarios and architecture dimensions and decisions, the overall design cycle time is greatly reduced."

The new Multicore Optimization Technology enables Platform Architect users to create task-driven workload models of the end-product application, known as task-graphs, enabling analysis and optimization of hardware/software partitioning and system performance. After hardware/software partitioning is finalized, architects reuse the same task-graphs and task-driven traffic for SoC-level architecture exploration and IP selection, as well as interconnect and memory subsystem performance optimization. Benefits include optimized multicore system performance, shorter evaluation times and faster time-to-market.

"Developers of multicore SoCs, chipsets and systems often tell us how worried they are about the risks of over-design and under-design, causing either uncompetitive products or expensive re-spins. They are realizing that multicore architecture analysis needs to be much more robust and start much earlier," says Frank Schirrmeister, director of product marketing, System-Level Solutions, Synopsys. "The new Multicore Optimization Technology for Platform Architect allows our users to find and resolve multicore performance issues while architecture changes are still feasible, avoiding costly re-work to hardware and software implementations."

Interaction between providers of hardware and software IP, multicore SoCs, chipsets and systems have become increasingly complex. Multicore Optimization Technology for Platform Architect greatly improves the effectiveness and precision of this collaboration by replacing written and verbal specifications with executable performance models of multicore system architectures. These can be easily shared between design chain partners without depending on final software and hardware.

Availability

Multicore Optimization Technology for Platform Architect is available effective immediately as an option for customers of Platform Architect. For more information on Platform Architect please visit <http://synopsys.com/platformarchitect>.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design,

verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

Synopsys is a registered trademark of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.
