# Synopsys' DesignWare DDR PHY Compiler Eases Integration of Memory Interface IP

GUI-Based Tool Enables Designers to Quickly Optimize DDR Memory Interface IP for Specific Applications

MOUNTAIN VIEW, Calif., Jan. 26, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the immediate availability of the DesignWare® DDR PHY compiler, supporting DDR2, DDR3, LPDDR and LPDDR2 SDRAMs. The DesignWare DDR PHY compiler offers designers a web-based GUI to assemble a customized, high-performance DDR PHY for their system-on-chips (SoCs). The DesignWare DDR PHY compiler evaluates more than 60 variables and allows the evaluation of unlimited 'what-if' scenarios. The output of the PHY compiler is a customized hard DDR PHY that is optimized for the target application.

"As a leading fabless design integrator, GUC is committed to delivering high-quality designs to our customers," said Dr. Keh-Ching Huang, head of Marketing and IP Solution Planning at Global UniChip. "Synopsys' DesignWare DDR PHY compiler has helped us resolve what has traditionally been a very complex and time consuming task. We have used the compiler to refine the DesignWare DDR PHY to reach our ideal PHY implementation, saving us significant time and effort."

Supporting the DesignWare DDR2/3-Lite, DDR 3/2 and DDR multiPHY IP products, the DesignWare DDR PHY compiler's GUI steps the user through a series of decisions as they construct their DDR PHY from hard IP components, including application-specific DDR I/Os. Designers have control over multiple variables including supported DRAM types (such as DDR3, DDR2, Mobile DDR and/or LPDDR2), foundry and process node, memory channel width, power-to-signal ratios, core power requirements and other physical placement variables. The DesignWare DDR PHY compiler produces an instantly viewable image of the DDR PHY layout, a list of the pins, area, a power consumption report, placement scripts and an RTL model of the PHY.

"The DDR interface is a crucial component of most SoCs, particularly the I/O ring, which can significantly impact the die size and power of the design," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "Synopsys developed the DesignWare DDR PHY compiler to address our customers' need for application-specific DDR PHYs that meet their aggressive power and area requirements."

Synopsys' comprehensive DesignWare DDR IP offering consists of digital controllers and PHY IP supporting DDR, DDR2, DDR3, Mobile DDR and LPDDR2. The DesignWare DDR PHY IP supports leading process technologies and includes a DFI 2.1-compliant interface. Synopsys' DesignWare Universal DDR Memory and Protocol Controller IP complement the DesignWare DDR PHY IP, offering a comprehensive DDR interface solution from a single IP vendor. Synopsys helps lower integration risk by providing high-quality DDR IP solutions that have been implemented in hundreds of applications and are shipping in volume production.

Synopsys will be demonstrating the DesignWare DDR PHY compiler at the upcoming DesignCon 2011 Conference (booth number 606) on February 2-3 at the Santa Clara Convention Center in Santa Clara, California.

**Availability**

The DesignWare DDR PHY compiler is available to licensed customers of select DesignWare DDR PHY IP today.

**About DesignWare IP**

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols, analog IP, embedded memories, logic libraries, embedded test & repair IP, audio post-processing software and configurable processor cores. In addition, Synopsys offers SystemC transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges

designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.



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