Synopsys Announces Immediate Availability of the DesignWare ARC Processor Core for Blu-ray Disc Players

DesignWare ARC AS 221 BD and 600 Family Enhancements Improve Overall System Performance, While Reducing SoC Power and Silicon Area

MOUNTAIN VIEW, Calif., Nov. 18, 2010 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the immediate availability of the DesignWare™ ARC™ AS 221 BD dual-core processor optimized for high-definition (HD) audio applications. In addition, Synopsys announced three new enhancements to its DesignWare ARC 600 32-bit configurable processor family, including an optional Memory Protection Unit (MPU), Power Management Unit (PMU) and single cycle 16x16 multiplier. The latest features allow designers to incorporate advanced functionality into their designs, while achieving higher performance, smaller area and lower power consumption. Used by more than 150 companies worldwide and shipped in more than 550 million ARC processor-based products annually, Synopsys' DesignWare ARC cores enable designers to lower integration risk and speed time-to-market for their embedded system-on-chip (SoC) designs.

The DesignWare ARC AS 221 BD dual-core processor is optimized for HD audio SoCs targeting Blu-ray Disc and Pulse Code Modulation (PCM) 192 kHz/24-bit digital audio streaming applications. This product extends Synopsys' DesignWare Sound-to-Silicon AS 200 processor family with a high-performance dual-core processor and a complete software stack with all the required codecs, media streaming framework, and Blu-ray Disc use cases. Including all the memories required to run the full Blu-ray software stack, the DesignWare ARC AS 221 BD dual-core processor occupies 0.81 mm2 in a 65-nm LP process, up to half the size of alternative solutions. The processor's power consumption, at 0.26 mW/MHz, is up to one-and-a-half to three times more power efficient than existing solutions.

The DesignWare ARC 600 family includes a full range of configurable and extensible 32-bit cores ranging from full-featured to ultra-compact configurations. All of the DesignWare ARC cores utilize a 16-/32-bit instruction set architecture (ISA) that provides both reduced instruction set computing (RISC) and full digital signal processing (DSP) in an easy to use, unified architecture. The latest enhancements to the DesignWare ARC 600 family provide designers with a richer feature set and the added flexibility to tailor the IP to their target application.

- The optional MPU for the DesignWare ARC 610D and 625D cores gives software running on the core the ability to control access rights to the memory. This improves performance by preventing a process running on the DesignWare ARC core from accessing memory that has not been allocated to it.
- The optional PMU for the DesignWare ARC 605, 610D and 625D cores allows application software control over clocking and voltage for the core, allowing dynamic power consumption management.
- The optional single-cycle 16x16 multiplier is available for the DesignWare ARC 601, 605, 610D and 625D cores. The new multiplier, an addition to the already available single- and multiple-cycle 32x32 multiplier configuration options, reduces power consumption and silicon area for applications that do not require the processing speed of a 32x32 multiplier.

"By providing the DesignWare ARC AS 221 BD processor core solution which delivers 3.5 giga operations per second with full support for the Blue-ray Disc audio stack, Synopsys is helping designers implement advanced high-definition audio functionality into their SoCs," said Joachim Kunkel, senior vice president and general manager for the Solutions Group at Synopsys. "Shipped in more than 550 million ICs annually, Synopsys' high-quality DesignWare ARC processor cores are trusted by designers to help them reduce integration risk and achieve the performance, power and area requirements of their advanced SoCs."

Availability

The DesignWare AS 221 BD and the new enhancement options to the DesignWare ARC 600 family cores are available now. For more information please visit: https://www.synopsys.com/designware-ip/processor-solutions/arc-processors.html .

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. In

addition, Synopsys offers SystemC transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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Editorial Contact:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900 x114
sbrennan@mcapr.com

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