Synopsys Enhances Synplify FPGA Synthesis Software With up to 4X Faster Runtime and New Team-Design Capabilities

New Release Also Delivers DesignWare Library IP Support for Production FPGA Designs

2010.09 Release Highlights:

-- Up to 4X synthesis runtime improvement

-- New global placer for quality of results improvements on existing designs

-- New team-design feature for concurrent design development

-- New support for DesignWare Library datapath and building block components for FPGA Implementation and ASIC Prototyping

MOUNTAIN VIEW, Calif., Sept. 27 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the availability of enhancements to its Synplify Pro® and Synplify® Premier FPGA synthesis tools. The new features in the 2010.09 release shorten logic synthesis runtimes and enable faster post-netlist incremental design turns. Comprehensive support for Synopsys DesignWare® Library datapath and building blocks components enables the use of common RTL from prototype to production. In addition, a unique team-design interface allows geographically distributed teams to work on portions of the design in parallel, accelerating logic synthesis performance and improving the quality of results (QoR) of their design.

"Designers increasingly require fast design turnaround, quick and accurate feedback on design performance and tools that improve the productivity of their geographically distributed design teams," said Ed Bard, senior director of marketing, Solutions Group at Synopsys. "We enhanced the latest releases of Synplify Pro and Synplify Premier with these requirements in mind. Designers implementing FPGAs for production applications or ASIC prototyping will benefit from the faster, easier-to-use Synplify-based design flows."

"As the leading provider of FPGAs, we are excited to see Synopsys' commitment to making their high quality DesignWare IP available to FPGA designers. Synchronized support for DesignWare Library will greatly improve user productivity in FPGA-based design flows," said Tom Feist, senior director of marketing for ISE Design Suite at Xilinx. "We have been working closely with Synopsys to ensure that our mutual customers gain the power efficiency, performance-capacity and price-performance of our Virtex-6, Spartan-6 and new 28nm 7 series FPGAs. The Synplify FPGA synthesis tools' new team-design flow, improved runtime speeds and high quality of results will be critical for large-scale designs with up to two million logic cells."

"The team-design features within the Synplify synthesis tool complement the incremental compilation technology in our Quartus II software in order to help users dramatically reduce design iteration times," said Phil Simpson, senior manager, software technical marketing and EDA relationships at Altera Corporation. "Customers leveraging these solutions to design with our Arria, Cyclone or Stratix FPGAs will achieve rapid design turn-around times with improved quality of results and higher levels of productivity."

The 2010.09 Synplify Pro and Synplify Premier product releases now offer synthesis support for SiliconBlue's iCE65 family of low-power FPGAs. Customers with active all-vendor configurations will receive support for these FPGAs at no additional cost.

"The adoption rate of our mobileFPGA devices is very strong, especially when you consider that many of our designers have never used FPGAs," said Kapil Shankar, CEO at SiliconBlue Technologies. "The Synopsys Synplify FPGA synthesis solution will further accelerate this rate by enabling these users to achieve very high quality of results with low area utilization quickly and easily, getting their mobile handsets to market as fast as possible."

Up to 4X Synthesis Runtime Improvement

Synplify Premier's FAST logic synthesis mode now offers up to a 4X speed improvement over traditional logic synthesis when using a single processor. The new compile- point technology enables additional speed improvements with automatic parallel timing-driven synthesis execution on different portions of a design to take advantage of computers with multiple processor cores.

Physical Synthesis with New Global Placer for Incremental Quality of Results Improvements

A new physical synthesis flow within Synplify Premier employs Synopsys' global placer technology to apply

performance improvements to an existing placed and routed design. Physical constraints are automatically determined from prior place and route runs. This makes the flow easy to use for logic synthesis users by freeing them from the need to perform complex physical constraint setup.

Team-Design Interface and Bottom-Up Flows allow Parallel Development

Both the Synplify Premier and Synplify Pro tools incorporate new team-design features for hierarchical project management and concurrent development. Design blocks, or previously verified design IP, can be created and shared internally. Floorplanning is not required, making this flow easy to use. Teams can now manage and review their design implementation results and synthesis settings for each block hierarchically. Design team members can take a snapshot of a block and transfer the design files to the team leader for overall integration into the design. Design blocks can be integrated at both the RTL or EDIF levels, saving time, locking in performance and ensuring predictable results.

Comprehensive DesignWare Library Support for FPGA-based Prototyping

Synplify Premier now supports the full suite of datapath and building block components within DesignWare Library. Synplify Premier users can now synthesize ASIC RTL that instantiates any of the DesignWare Library's components to create FPGA-based prototypes of their ASIC design and achieve performance-optimized results. ASIC and FPGA component support are now synchronized to help ensure the same DesignWare Library component used in the prototype is also used in the ASIC.

Availability

The 2010.09 release of the Synplify Pro and Synplify Premier products is available now and can be obtained directly from Synopsys through SolvNet by existing customers under maintenance. The Synplify FPGA synthesis products are supported on Windows and Linux, 32 and 64-bit platforms.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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