MEDIA ADVISORY/ALERT: Synopsys Showcases DesignWare IP Solutions for PCI Express, USB and SATA at Intel Developer Forum 2010

SAN FRANCISCO, Sept. 10 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, will be demonstrating its complete DesignWare® IP solutions for PCI Express® 3.0, USB 3.0 and SATA 6 Gb/s, consisting of device, host, PHY and verification IP, at the Intel Developer Forum (IDF) in San Francisco, California from September 13-15.

IDF is the premier global technology industry event bringing together technology professionals who are actively directing where technology is going. At IDF, attendees can experience visionary keynotes, technology and industry insights, and technical sessions (including lectures, interactive panels, hands-on labs and Hot Topic Q&As). There is also a packed technology showcase with exhibits and demonstrations from Intel and leading technology companies.

WHAT: Synopsys will be showcasing its latest developments in DesignWare IP for PCI Express 3.0, USB 3.0 and SATA 6 Gb/s at IDF in the USB and General Communities.

WHEN: September 13-15

WHERE: Moscone Center West, 800 Howard Street, San Francisco, CA 94103

TECHNOLOGY SHOWCASE HOURS:

Monday, September 13, 5:00pm-7:00pm

Tuesday, September 14, 11:00am-1:00-pm & 4:00pm-7:00pm

Wednesday, September 15, 11:00am-2:00pm

Synopsys Highlights at IDF

General Community:

Synopsys Booth #313

- Synopsys DesignWare Digital IP for PCI Express 3.0

  This demonstration incorporates the DesignWare IP for PCI Express 3.0 to create designs for a PCI Express 3.0 root complex and endpoint. These two designs are connected via a backplane and a logic analyzer is used to verify the PCI Express 3.0 traffic running at 8 GT/s between the two devices.
- Synopsys DesignWare SATA 6 Gb/s Demo

  This demonstration incorporates the DesignWare IP for SATA 6 Gb/s digital controller and PHY to create designs for Solid State Devices (SSD). The SATA-based SSD design is implemented on Synopsys' HAPS FPGA-Based prototyping solution and demonstrates a fully functional SATA 6 Gb/s SSD interoperating with a commercially available SATA 6 Gb/s Host capable PC.

LeCroy Booth #952

- LeCroy and Synopsys Showcase PCI Express 3.0 Interoperability

  Through a design-under-test (DUT) that uses the DesignWare IP for PCI Express 3.0, this demonstration utilizes the LeCroy's Summit T3-16 Protocol Analyzer, Summit Z3-16 Protocol Exerciser and the Summit Z3-16 Test Platform to test a PCI Express 3.0-based design for compliance to the current PCI Express 3.0 specification.

Agilent Booth #418

- Agilent and Synopsys Enable PCI Express 3.0 Ecosystem

  Based on a DUT that implements the DesignWare IP for PCI Express 3.0, this demonstration uses Agilent's complete test solution for PCI Express 3.0 (including a Protocol Analyzer and Exerciser for PCIe 3.0) and the Digital Test Console to check for interoperability of multiple PCI Express 3.0 devices.

To view DesignWare IP for PCI Express 3.0 interoperability videos, click here.

USB Community

Synopsys Booth #943

- *DesignWare SuperSpeed USB Complete Solution Demonstrations*

  This series of demonstrations will feature the industry's only complete, single-vendor SuperSpeed USB 3.0 solution, consisting of controllers, PHY and verification IP. Synopsys will showcase its DesignWare USB 3.0 xHCI Host and USB 3.0 Device Controllers operating with off-the-shelf USB 3.0 and USB 2.0 products displaying high-definition video running at hundreds of megabytes per second. Additionally, the demonstration will show proven interoperability of the DesignWare USB 3.0 PHY and DesignWare USB 3.0 host with device controllers implemented on HAPS® FPGA boards with MCCI Drivers.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare® IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable CPU/DSP cores. In addition, Synopsys offers SystemC transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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