

# Synopsys Announces Immediate Availability of DesignWare MIPI M-PHY IP in 40-nm Process Technology

## DesignWare DigRF v4 Controller and M-PHY IP Address Demand for Higher Throughput in LTE and WiMAX Mobile Devices

MOUNTAIN VIEW, Calif., Aug. 24 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced immediate availability of the DesignWare® MIPI M-PHY® IP for next-generation high-speed interfaces based on the newly ratified MIPI® Alliance M-PHY specification. With this latest addition to the [DesignWare MIPI IP portfolio](#), Synopsys is the first provider to offer a comprehensive solution of a controller and PHY IP for both the MIPI DigRF(SM) v3 (2.5G/3.0G) and v4 (4G) standards. Incorporating both standards in a mobile device brings the benefit of the faster 4G standards while preserving broad coverage by using 2.5G/3.0G as a fallback mode. The configurable MIPI DigRF V4 Master Controller and M-PHY hard macro are compliant to the MIPI Alliance specifications. Utilizing a single-vendor solution enables designers to lower the risk and cost of integrating these MIPI interfaces into baseband and application processor integrated circuits (ICs), speeding time-to-market of advanced semiconductor solutions for LTE and Mobile WiMAX.

The DesignWare MIPI M-PHY implements all required physical layer functionality defined in the MIPI DigRF v4 specification. The DesignWare MIPI M-PHY is designed to meet the stringent power consumption guidelines of the MIPI M-PHY specification, keeping the energy expenditure below 15pJ/bit for typical LTE applications. The integrated analog Phase Lock Loop (PLL) and biasing block are designed to help guarantee the integrity of the high-speed clocks and signals required to meet the strict timing requirements of the protocol, affording designers a robust and low risk solution. In addition, the DesignWare MIPI M-PHY supports the optional dithering functionality defined in the MIPI DigRF v4 specification to further lower Electromagnetic Interference (EMI).

"As an active contributor to the MIPI working groups, Synopsys continues to make solid contributions that support the MIPI Alliance portfolio of specifications," said Joel Huloux, chairman of the MIPI Alliance. "Synopsys is speeding the adoption of the new M-PHY interface into mobile devices and helping designers benefit from the latest functionality offered by the MIPI-based technology."

"To address the growing usage of multimedia content in mobile devices, designers are using standards-based interfaces from the MIPI Alliance to help them meet the increased data throughput requirements for mobile terminals targeting 4G standard air interfaces," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "Synopsys is playing a key role in supporting the MIPI ecosystem by providing designers with high-quality DesignWare MIPI IP consisting of DigRF v3/v4, CSI-2, D-PHY, and M-PHY IP, enabling them to lower the risk of integrating MIPI interfaces into their designs."

### Availability

The DesignWare MIPI M-PHY is available now in leading 40-nanometer process technologies. The DesignWare MIPI IP for DigRF v3/v4, CSI-2 and D-PHY are available now. For more information, visit: <http://www.synopsys.com/mipi>.

### About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, Ethernet, HDMI, and MIPI DigRF v3/v4, CSI-2, M-PHY and D-PHY. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Touch Screen Controllers and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: <http://www.synopsys.com/designware>. Follow us on Twitter at [http://twitter.com/designware\\_ip](http://twitter.com/designware_ip).

## **About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

## **About MIPI Alliance**

MIPI (MIPI®) Alliance is a global, collaborative organization comprised of companies spanning the mobile ecosystem that are committed to defining and promoting interface specifications for mobile devices. MIPI Specifications establish standards for hardware and software interfaces which drive new technology and enable faster deployment of new features and services across the mobile ecosystem.

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