Synopsys Galaxy Implementation Platform Used by TSMC for 28nm Process

Product Qualification Vehicle Test Chip Tapeout Includes Advanced Routing Rules, Low Power and Signoff Capabilities

MOUNTAIN VIEW, Calif., Aug. 9 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that TSMC has successfully taped out a complex 28-nanometer (nm) Product Qualification Vehicle (PQV) test chip using Synopsys' Galaxy™ Implementation Platform. Key features used to design the PQV test chip include 28-nm design rule support for place-and-route, interconnect process modeling, IEEE 1801-2009 (UPF)-based hierarchical low power flow, power-aware design-for-test (DFT) and advanced signoff capabilities. Synopsys tools exercised by TSMC in the RTL-to-GDSII implementation and signoff flow for this test chip development included DC Ultra™ RTL synthesis, IC Compiler physical implementation, PrimeTime® SI timing signoff and StarRC™ Ultra parasitic extraction.

TSMC's complex 28-nm test chip design consisted of more than 200 million gates of logic and memory combining multiple IP cores and custom designed blocks. The chip's multiple power and clock domains presented additional design challenges that were efficiently handled by the Galaxy platform tools. TSMC deployed advanced methodologies during the test chip design to address hierarchical power implementation, DFT, advanced routing rules and manufacturability compliance. To address the design's multiple multi-voltage blocks, TSMC utilized the Galaxy platform's hierarchical low power flow, including power intent definition described with UPF. This approach enabled the engineering team to implement different sub-blocks of the design concurrently, resulting in faster overall time-to-results. In addition, the Galaxy tools were used to successfully deploy TSMC's pulsed latch approach to maximize power savings across the chip. To validate 28-nm manufacturing compliance, TSMC used Synopsys' IC Compiler Zroute DFM-aware routing capabilities.

"We continuously work with Synopsys to identify EDA and manufacturing solutions that address the challenges of the latest advanced semiconductor processes," said ST Juang, senior director of design infrastructure marketing at TSMC. "As a result of our PQV test chip design project, we have successfully used Synopsys' Galaxy Implementation Platform in our 28-nanometer process, including capabilities for hierarchical low power implementation, routing rules and manufacturing compliance. We appreciate Synopsys' on-going collaboration during our aggressive process development and deployment projects that allow us to deploy our solutions to our common customers in a very timely manner."

"As semiconductor process technologies continue to increase in complexity it is essential for industry leaders like TSMC and Synopsys to engage at deep technical levels," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Through the Galaxy Implementation Platform collaboration with TSMC on its advanced 28-nanometer PQV test chip project, our customers can be assured that the Galaxy Platform can be used successfully in this new technology. This will enable predictable silicon success as they embark on their next design projects."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon

verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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