Synopsys DesignWare DDR multiPHY IP Supports Six DDR Standards in a Single PHY

New DDR multiPHY Allows One Chip to Target Multiple Applications

MOUNTAIN VIEW, Calif., April 7 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced availability of the DesignWare™ DDR multiPHY which is designed to support a broad range of DDR SDRAM standards in a single PHY without sacrificing power consumption or silicon area. These standards include LPDDR2, LPDDR/Mobile DDR, DDR3, DDR3L (1.35 V), DDR3U (1.2x V), and DDR2. The DesignWare DDR multiPHY enables designers to target different DDR types for a single chip through simple software control. This capability makes it extremely flexible to integrate into an extensive array of applications such as consumer electronics, mobile, networking, server, computing, commercial/industrial and automotive applications. The DesignWare DDR multiPHY supports data rates from 0 to 1066 Mbps and offers a DFI 2.1 compliant interface to the memory controller.

"Memory interfaces continue to be one of the key IP requirements we see in chip development. New standards such as DDR3, DDR3L and LPDDR2 are designed to meet system performance requirements while utilizing less power," said Dr. Keh-Ching Huang, Head of Marketing and IP Solution Planning at Global Unichip. "By supporting all facets of the DDR standards, Synopsys' unique DesignWare DDR multiPHY enables us to quickly incorporate the necessary functionalities into our SoC designs with less risk."

The DesignWare DDR multiPHY is architected for extremely low power consumption and features Delay Lock Loop (DLL) bypass modes for operation below 200 MHz. It also features an I/O retention mode that allows the chip's power supplies to be shut down completely while a small number of I/Os remain powered on to keep the external SDRAMs in self refresh mode. The DesignWare DDR multiPHY is designed to support the anticipated DDR3U standard operating at 1.2 or 1.25 V. Additionally, the DesignWare DDR multiPHY provides built-in data training circuits to enable in-system calibration, providing optimized system-level timing without material interaction with the memory controller.

The DDR multiPHY is a hard macro similar to Synopsys' complementary DDR PHY offerings. Hard DDR PHYs offer significant benefits over "soft" PHYs or all digital PHYs such as:

- Quick integration. All pieces of the PHY come from one vendor and have been verified together
- Minimal timing closure problems. Known performance, proven in silicon
- Better performance margins. Lower jitter, better duty cycle and more supply noise rejection
- Area optimized circuits. Each bit path is designed with matched flight times on the data buses

"It has become as important to minimize power as it has to minimize overall chip cost in portable electronics," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "The DesignWare DDR multiPHY not only offers designers the flexibility to utilize any DDR SDRAM in the system through simple software control, it also features a power-conscious design that minimizes the silicon area and cost."

The DesignWare DDR multiPHY is a part of Synopsys' comprehensive DesignWare DDR IP offering that consists of digital controllers and PHY IP supporting DDR, DDR2, DDR3, Mobile DDR and now LPDDR2. The comprehensive portfolio of DDR IP supports leading 130-nm, 90-nm, 65-nm, 55-nm and 45/40-nm technologies. Synopsys helps lower integration risk by providing high-quality DDR IP solutions that have been implemented in hundreds of applications and are shipping in volume production.

Availability

The DesignWare DDR multiPHY is available now. For more product information and video demonstrations of DesignWare DDR IP, visit: http://www.synopsys.com/ddr

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, Ethernet, HDMI and MIPI IP including 3G DigRF, CSI-2 and D-PHY. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Touch Screen Controllers and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development

of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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