

Synopsys Announces DesignWare Protocol Analyzer for Verification of SuperSpeed USB 3.0-based Designs

New Verification IP Capability Speeds Time-to-Market by Simplifying Debug of USB 3.0 Interfaces

PRNewswire

MOUNTAIN VIEW, Calif.

(NASDAQ-NMS:SNPS)

MOUNTAIN VIEW, Calif., Jan. 13 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the DesignWare® USB 3.0 Protocol Analyzer, a new graphical debugger for SuperSpeed USB 3.0, the latest generation of the USB interface that delivers 10 times the speed of Hi-Speed USB 2.0. The DesignWare USB 3.0 Protocol Analyzer simplifies debug for engineers verifying SuperSpeed USB 3.0 and USB 2.0 interfaces in their systems-on-chip (SoCs) by providing a graphical view of the protocol traffic. It helps users quickly identify unexpected patterns in the design traffic and then switches to a detailed view of the packet information to determine the cause.

The DesignWare USB 3.0 Protocol Analyzer is part of the DesignWare verification IP for USB 3.0. It displays the protocol traffic generated from simulation runs using the DesignWare USB 3.0 verification IP transactors in a high-level color-coded summary view and a more detailed symbol-view of the individual packets and payloads. Debug is accelerated by allowing designers to easily distinguish and browse traffic types and switch between the two views. The DesignWare Verification IP for USB 3.0 supports Verilog testbenches, and constrained random methodologies as defined in the proven *Verification Methodology Manual (VMM) for SystemVerilog*.

"The DesignWare Protocol Analyzer allows us to browse protocol activity and makes it much faster and easier to debug protocol errors and latency issues," said Jessy Chen, executive vice president of Realtek. "As we develop and bring SuperSpeed USB 3.0 integrated products to the market, it is important that our engineers have the right tools to accelerate investigation of protocol behavior."

"Verification engineers are faced with tremendous challenges as standard interfaces on SoC designs increase in number and complexity," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "By easing the verification effort with the new DesignWare Protocol Analyzer, Synopsys is leading the effort to help Realtek and other early providers of USB 3.0 solutions bring innovative products to market faster and with less risk."

Availability

The DesignWare USB 3.0 Protocol Analyzer and DesignWare USB 3.0 Verification IP are both available now with VCS® support to select customers. For more information, please visit: <http://www.synopsys.com/usb3>

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, HDMI, MIPI and Ethernet. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Touch Screen Controllers and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: <http://www.synopsys.com/designware>.

Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

Synopsys, DesignWare and VCS are registered trademarks of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:

Sheryl Gulizia
Synopsis, Inc.
650-584-8635
sgulizia@synopsys.com

Karen Do
MCA
650-968-8900 x111
kdo@mcapr.com

SOURCE: Synopsys, Inc.

Web site: <http://www.synopsys.com/>
