TSMC Selects Synopsys HSIM Simulator for Sub-40nm Memory IP Characterization

Accuracy, Performance and Capacity Cited as Key Decision Factors

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MOUNTAIN VIEW, Calif., Sept. 14 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that TSMC has adopted Synopsys' HSIM® hierarchical FastSPICE circuit simulator for its sub-40-nanometer (nm) memory intellectual property (IP) characterization flow. The HSIM simulator will be deployed for TSMC advanced SRAM compilers for timing, power simulation, dynamic IR drop and EM analysis, as well as for full-chip simulation with extracted package models. Using the latest version of the HSIM tool, TSMC is able to improve memory characterization throughput by 10 times while achieving tight correlation to silicon measurements.

"At 40-nanometer nodes and beyond, post-layout parasitic data, power reliability and leakage need to be accounted for when characterizing memories," said ST Juang, senior director of Design Infrastructure Marketing at TSMC. "We had adopted HSIM for our memory IP characterization at previous technology nodes, and after extensive evaluation we chose HSIM for our sub-40-nanometer flow based on its advanced technologies for post-layout analysis and its ability to deliver accurate simulation results while maintaining fast throughput for our largest memory compilers."

As layout geometries shrink, accurate characterization of memories becomes more of a challenge. Previous methodologies that have employed critical path and cut netlists are no longer adequate to accurately verify the impact of cross-coupling effects and layout parasitics. As a result, more customers have adopted the method of verifying the entire memory design, including the chip packaging, for sub-40nm process nodes. HSIM, the technology-leading FastSPICE circuit simulator, addresses this challenge by delivering accurate simulation results with superior performance. HSIM provides a comprehensive solution for circuit simulation, post-layout analysis, reliability analysis and electrical rule checking.

"TSMC's selection of HSIM for their most advanced memory IP characterization validates our continued R&D investment in circuit simulation technologies," said Paul Lo, senior vice president and general manager of the Analog/Mixed-Signal Group at Synopsys. "Through collaboration with companies like TSMC, we are able to deliver solutions for our customers' toughest circuit verification challenges."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan,

Asia and India. Visit Synopsys online at http://www.synopsys.com.

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