Synopsys Introduces Galaxy 2009 with 2x Faster Throughput

Platform Delivers Breakthrough Design Implementation and Signoff Productivity with New Multicore Performance and Multi-corner/Multi-mode Technologies

PRNewswire
MOUNTAIN VIEW, Calif.
(NASDAQ-NMS:SNPS)

MOUNTAIN VIEW, Calif., July 28 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today introduced the latest release of its Galaxy™ Implementation Platform delivering 2x faster design implementation and signoff throughput with new multicore performance and multi-corner/multi-mode (MCMM) technologies. Built-in support for multicore processing across the Galaxy Platform enables engineering teams to immediately boost runtime performance using their existing compute servers. Additionally, the Galaxy Platform includes new MCMM technology providing improved quality of results and faster design closure when using a combined Design Compiler® Graphical and IC Compiler flow. The Galaxy 2009 release is available now.

In March 2008, Synopsys announced a broad multicore initiative to deploy advanced parallel, threaded and other optimized compute technologies across its verification, implementation and manufacturing platforms to reduce time-to-results. The most recent result of this initiative is the expansion of the Galaxy Platform with multicore technology to deliver 2x faster performance for design implementation and signoff. Multicore technologies being introduced today with the Design Compiler synthesis, TetraMAX® automatic test pattern generation (ATPG), IC Compiler place-and-route, IC Validator physical verification, Star-RCXT™ extraction and PrimeTime® static timing analysis solutions deliver breakthrough productivity and faster design closure. Measurable performance improvements deploying these technologies include:

- Design Compiler: 1.5x faster runtime with four processor cores
- IC Compiler: 2.5x faster runtime with MCMM using four cores
- Star-RCXT: 3x faster performance using four cores and 8x faster using 16 cores
- PrimeTime: 50 percent faster, on average, for typical production flows compared with the previous release. In addition, a faster run mode in PrimeTime ideal for early signal integrity analysis delivers 2x faster runtime, on average.
- TetraMAX: 3x faster performance with four cores and 6x faster performance with eight cores
- IC Validator: near-linear scalability with 7x speedup using eight cores and 20x speedup using 25 cores.

New MCMM synthesis technology in Design Compiler Graphical, a component of Synopsys' Eclypse™ Low Power Solution, supports concurrent optimization for worst-case leakage and timing corners. Design Compiler uses a common multi-scenario definition with IC Compiler. Actual design results have shown 10 percent lower leakage when using MCMM optimization with a combined Design Compiler and IC Compiler flow. PrimeTime's Distributed Multi-Scenario Analysis (DMSA) capability has been extended to deliver a more comprehensive set of engineering change orders (ECOs) for both setup and hold timing violations, thus minimizing late-stage iterations in the design process.

"With the increasing complexity and diversity of system-on-chip designs, faster, unified implementation solutions are essential," said Bijan Kiani, vice president of product marketing, Design and Manufacturing Products, at Synopsys. "Galaxy 2009 delivers faster runtime performance with comprehensive multicore and MCMM support for better quality of results and faster design closure. As a result, engineers are able to achieve higher productivity on their most challenging designs."

Galaxy Implementation Platform

The Galaxy Implementation Platform is a comprehensive solution for cell-based and custom IC implementation. Galaxy accepts design intent in industry standard formats and generates a production-ready IC design in GDSII format. Galaxy RTL and physical implementation concurrently balance design constraints by performing intelligent tradeoffs between speed, area, power, test and manufacturability. Galaxy signoff engines accurately model complex physical interactions to ensure signal and power integrity. Coherent algorithms for parasitic extraction and timing produce correlated results.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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