Aquantia Deploys Synopsys IC Validator and IC Compiler for 40nm Quad 10GBASE-T Design

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In-Design Physical Verification Key to Accelerated Manufacturing Compliance

MOUNTAIN VIEW, Calif., June 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Aquantia, the leading innovator in 10GBASE-T networking, has deployed Synopsys' recently announced IC Validator, the newest addition to the Galaxy™ Implementation Platform, into production use at 40 nanometers (nm). IC Validator is an ideal add-on to IC Compiler for In-Design physical verification, enabling place and route engineers to accelerate time to tapeout and improve manufacturability by enabling physical verification within the implementation flow. Compared to the typical implement-then-verify flow, the In-Design flow is instrumental in avoiding late-stage surprises and enabling integrated circuit (IC) providers like Aquantia - which is in the process of delivering an advanced 40nm-based quad 10GBASE-T solution - to achieve a faster, robust hand-off to the foundry.

"A few weeks can mean the difference between meeting or missing the market window in our fast moving market," said Ramin Shirani, vice president of engineering at Aquantia. "IC Validator's ability to perform In-Design physical verification within IC Compiler reduces the physical verification effort from weeks to days by automating and accelerating one of the most onerous parts of our design cycle. We were impressed by IC Validator's fast convergence in concurrently implementing signoff metal-fill and DRC while reducing the timing impact of such implementation."

Prevailing physical verification flows are predominantly post-processing oriented, relying on modifications to the design after GDSII has been generated. These flows can lead to suboptimal results and can induce multiple discover-then-fix iterations. Metal-fill insertion, a mandatory manufacturability step at the advanced nodes, exemplifies this issue. Physical designers stream out the timing-closed, post-fill design for signoff validation and then stream it back in to fix any signoff errors flagged during physical verification. This time-intensive discover-then-fix loop is typically repeated on each block until the post-fill design is both signoff qualified and timing clean.

With In-Design physical verification, IC Validator and IC Compiler address the manufacturability issues within the place and route environment. The seamless integration enables an optimal metal-fill flow that is timing aware, signoff quality and void of expensive stream-outs and stream-ins. Additionally, this flow achieves higher density by utilizing a track-less approach.

While In-Design physical verification is enabled through tight integration with place and route, it is founded on a high-performance, foundry-endorsed, signoff-accurate engine in IC Validator. With a native multicore architecture, IC Validator can significantly accelerate the metal-fill process by up to 20 times. For incremental fixes to metal fill near critical nets or ECOs, the In-Design flow enables rule-based, layer-based and area-based metal fill removal and re-insertion, thereby helping eliminate the need for costly full-chip runs.

"In-Design physical verification with IC Validator and IC Compiler is successfully addressing the increasing design-for-manufacturability needs of our customer base," said Saleem Haider, senior director of marketing, physical design and DFM at Synopsys. "For meeting foundry-dictated manufacturing needs, Aquantia's adoption of IC Validator demonstrates the value of placing the emphasis on the 'D' in DFM and handling manufacturability requirements during design instead of post-design modifications."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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