Tego Standardizes on VMM and Synopsys VCS Solution to Speed Verification of Radio Frequency Identification Tags

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VMM Verification Methodology Enables First-pass Silicon Success on World's First High-memory, Passive Tag Technology

MOUNTAIN VIEW, Calif., April 28 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced that Tego, Inc. has standardized on the production-proven VMM verification methodology and VCS® functional verification solution, both key components of Synopsys' Discovery™ Verification Platform, to verify their radio frequency identification (RFID) tags for the aviation industry. Tego's RFID tags, which are used to store intelligent data directly on an object without the need for battery power, have grown increasingly complex due to memory limitations and, therefore, require a robust verification solution to accelerate the design cycle. Tego chose a VMM-based approach to address the increased chip complexity, higher test volume and ease-of-use requirements. They have also standardized on the VCS solution to optimize performance, bug detection and capacity. The combined solution enabled Tego to achieve first-pass silicon success on its next-generation passive RFID tag and will help the company to hit ever-narrowing time-to-market windows on future projects.

"Complex designs require a scalable verification methodology that offers language compliance, interoperability and debug productivity, while also providing a very high level of performance that speeds time-to-market," said Bob Hamlin, chief technology officer at Tego, Inc. "VMM fulfills all of these key target requirements. We have embraced and successfully deployed the expanded VMM methodology and VCS on the merits of the solution's ability to enable rapid debug and fast design turns, all in an easy-to-adopt package."

A major benefit of VMM-based verification environments is easier customization. With VMM, Tego is now able to create a customized, "plug-and-play" testbench environment that can run data collection and comparison separately. Engineers are able to generate specific corner scenarios or collect functional coverage for particular test scenarios and generate new test cases without having to modify the entire testbench unnecessarily. Additionally, the VMM-based environment allows reuse of the pre-existing golden reference model, initialization routines and protocol-dependent monitoring logic, improving productivity and streamlining time-to-market for future designs.

"Tego is working on innovative, cutting-edge designs that require a powerful verification solution to ensure first-pass silicon success," said Swami Venkat, senior director of Marketing in the Verification Group at Synopsys. "We continue to invest in efficient and reusable verification methodologies and high-performance engines that help our customers accomplish their goals while accelerating time-to-market. Tego joins a growing list of companies who have incorporated VMM into their VCS-based functional verification flow."

About VMM

The VMM methodology enables chip development teams to use SystemVerilog to create comprehensive verification environments using transaction-level, coverage-driven, constrained-random and assertion-based techniques, and specifies library building blocks for interoperable verification components. The VMM methodology has been proven in production by hundreds of SoC and silicon IP verification teams around the world. In addition to the VMM base class library and applications, a variety of useful resources that help improve productivity for both new and existing VMM users are available at http://www.vmmcentral.org. The VMM for Low Power (VMM-LP) extends the VMM methodology for designs that employ aggressive power management techniques; the VMM-LP book is available for download at http://www.vmmcentral.org/vmmlp.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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