Synopsys Delivers 2x Verification Speed-up With VCS Multicore Technology

PRNewswire
MOUNTAIN VIEW, Calif.
(NASDAQ-NMS:SNPS)

New Technology Optimizes Verification Performance on Multicore CPUs

MOUNTAIN VIEW, Calif., April 6 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today unveiled new multicore technology within the VCS® functional verification solution, a key component of Synopsys' Discovery™ Verification Platform. VCS multicore technology delivers a two-times (2x) improvement in verification performance by harnessing the power of multicore CPUs. The new technology removes performance bottlenecks and speeds verification by distributing time-consuming activities across multiple cores. VCS multicore technology combines the speed-up from parallel computation with the industry-leading Native Testbench (NTB) compiler to meet the performance requirements for the verification of large-scale designs. This enhancement helps verification teams address the growing challenges of verifying increasingly complex designs and achieving first-pass silicon success.

"We continue to benefit from the innovative optimizations delivered by VCS," said Paul Tobin, director of Verification Center of Expertise at AMD. "As our engineers integrate more cores and deliver designs with an optimal balance of performance, power and virtualization, our verification teams rely on the speed-up delivered by VCS multicore to quickly verify these complex designs on Quad-Core AMD Opteron processors in our server farm."

Application and Design Parallelism

SystemVerilog adoption increased the deployment of advanced technologies such as constrained-random testbenches, assertions and coverage. Synopsys pioneered NTB optimization and delivered 5x faster performance on single-core CPUs by natively compiling these technologies. With the new multicore technology, the VCS solution extends the NTB optimization to run on multicore CPUs and parallelizes the entire verification environment to maximize performance. This includes the design under test as well as verification applications such as testbench, assertion, coverage and debug. Design-level parallelism (DLP) allows a user to concurrently simulate multiple instances of a core, several partitions of a large design, or a combination of the two. Application-level parallelism (ALP) allows users to run testbenches, assertions, coverage and debugging concurrently on multiple cores. The combination of DLP and ALP optimizes VCS performance over multicore CPUs.

"Synopsys continues to develop and deliver innovative optimizations to push the performance curve," said Manoj Gandhi, senior vice president and general manager, Verification Group, Synopsys. "VCS multicore technology builds on the already successful Roadrunner, Radiant and Native Testbench optimization and addresses the rapidly growing demands of modern verification. The new technology creates a foundation on which Synopsys will deliver even more innovations for multicore computing platforms."

Availability

The multicore technology in the VCS functional verification solution is available now in Beta and is expected to be in production in calendar Q3 of 2009.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and

manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected production date and benefits of multicore technology within the VCS functional verification solution. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2008, and subsequent forms 10-Q, entitled "Risk Factors."

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900 x114
sbrennan@mcapr.com

SOURCE: Synopsys, Inc.

Web site: http://www.synopsys.com/