Synopsys USB 2.0 PHY IP for Advanced 40-Nanometer Process First to Pass USB-IF Certification

High-Quality, Silicon-Proven DesignWare IP Lowers Design Risk and Enables Interoperability with Hi-Speed USB Products

MOUNTAIN VIEW, Calif., Dec. 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced that its DesignWare® USB 2.0 nanoPHY is the first 40-nanometer (nm) USB 2.0 PHY IP to successfully pass the USB Implementers Forum Hi-Speed USB PHY certification. Synopsys' technology-leading USB 2.0 nanoPHY mixed-signal IP, now available in a native 1.8V architecture, meets the full USB 2.0 specification including 5V short tolerance for 24 hours and 3.3V operation. This architecture helps designers embed the DesignWare USB 2.0 PHY IP into system-on-chips (SoCs) utilizing the most advanced process geometries without compromising performance or long-term reliability.

The DesignWare USB 2.0 nanoPHY IP is designed for a broad range of high-volume mobile and consumer applications where the key requirements include minimal area, minimal dynamic and leakage power consumption. In addition, the DesignWare USB 2.0 nanoPHY IP has built-in tuning circuits designed to enable quick, post-silicon adjustments to account for unexpected chip/board parasitics or process variations, without having to modify the existing design. This allows designers to increase yield and minimize the cost of expensive silicon re-spins.

The DesignWare USB 2.0 nanoPHY IP is part of Synopsys' complete DesignWare USB 2.0 IP solution consisting of, digital controllers, PHY and verification IP. Synopsys offers a comprehensive portfolio of USB 2.0 IP for 180-nm, 130-nm, 90-nm, 65-nm, 45-nm, and now 40-nm process technologies. The DesignWare USB 2.0 IP products have been implemented in hundreds of USB applications and are shipping in high volume production.

"Certification is important because it demonstrates that IP solutions meet USB-IF interoperability standards and are compliant to the USB 2.0 specification," said Jeff Ravencraft, USB-IF president and chairman. "The availability of Synopsys' certified USB 2.0 PHY IP in the 40-nanometer process technology enables designers to quickly introduce next-generation Hi-Speed USB products including smart phones and mobile internet devices (MIDs) to the market."

"As the leader in USB IP, Synopsys provides designers with comprehensive, high-quality USB IP solutions that are silicon-proven and certified," said John Koeter, vice president of marketing, Solutions Group at Synopsys. "Being first to achieve USB 2.0 certification with a native 1.8V architecture is an important technical milestone, enabling the continued integration of USB 2.0 PHY IP using today's 40-nanometer processes and future 32-nanometer and 28-nanometer processes."

Availability

The logo-certified DesignWare USB 2.0 nanoPHY IP for the 40-nm process is available now. Please contact Synopsys for specific foundry support. The complete DesignWare USB 2.0 IP solution, consisting of PHY IP (ranging from 180-nm to 40-nm), digital controllers and verification IP, is also available today. For more information on DesignWare USB IP or to take a virtual tour of the Synopsys USB IP lab, please visit: http://www.synopsys.com/designware.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and

manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

Synopsys and DesignWare are registered trademarks of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA
650-968-8900 x115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

Web site: http://www.synopsys.com/
http://www.synopsys.com/designware/