VMM Users Drive New Features in Expanded Release

Enhancements to Industry's Most Proven Verification Methodology Include New Base Classes and Performance Analyzer Application

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MOUNTAIN VIEW, Calif., Dec. 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced the release of an expanded version of VMM, the industry's most production-proven verification methodology. The updated release includes new, user-driven features, such as a multi-stream scenario generator, transactor iterator and command-line options manager. These features increase scalability from block to system-level, ease-of-use and verification productivity. A new Performance Analyzer application further improves productivity by enabling analysis of shared design resources. The enhancements to VMM streamline the development of today's increasingly complex verification environments.

"After a thorough evaluation of competing verification methodologies, we standardized on VMM to streamline verification of our IP and microcontrollers," said Sury Maturi, director of the Design Automation Group at National Semiconductor. "The new, expanded release of VMM includes a number of enhancements that will allow us to further reduce our verification cycles, such as the multi-stream scenario generator and new test structure, which enables us to create sophisticated controllable scenarios and, consequently, achieve greater scalability and reuse of stimulus."

"As an international provider of high-end functional verification consulting services, we have deployed VMM for our clients on a range of projects across the globe," said Jason Sprott, vice president of Consulting at Verilab. "Because of our significant level of hands-on experience with verification methodologies, we were in an excellent position to help guide the evolution of VMM and contribute to the enhancements in the latest release. It now enables even higher levels of scalability, simplifies implementation and is more capable than ever at helping design teams accelerate the verification process."

"A robust and production-proven methodology is a must in order to meet today's demanding project schedules, and a strong ecosystem is equally important for ease-of-adoption," said Michael Hoyt, president and chief executive officer of Paradigm Works. "VMM not only delivers the strongest ecosystem in the industry, it also offers a suite of extremely useful applications. We have been and will continue to be part of this growing ecosystem focused on delivering applications that improve verification productivity."

Increased Scalability

The new release of VMM includes a multi-stream scenario generator, which increases block to system-level scalability by enabling users to layer and control the multi-stream scenarios hierarchically. It provides an easy way to generate, control and schedule different heterogeneous transaction sequences. The execution of multi-stream scenarios creates coordinated stimulus on multiple channels anywhere in the verification environment.

Enhanced Ease-of-use

With VMM's new transactor iterator, users can now configure multiple transactors in an identical fashion using the same amount of code it takes to configure a single transactor, simplifying the transactor configuration process. Additionally, a new command-line options manager simplifies the task of managing

complex verification environments within cross-functional teams by making it easier to check for run-time command-line options or options set through a set of option files.

Improved Productivity

A new application called Performance Analyzer now provides the ability to measure statistical functional coverage metrics, such as the utilization of shared resources, the response time of arbiter or slave devices, or the processing time of a functional block. The performance data can be queried and computed from multiple simulation results and performance metrics reported textually or graphically.

The latest release of VMM offers a new base class that enables test writers to compile and elaborate all tests at once then select, at run-time, which test to execute. This eliminates the need for a recompile of each test, thereby speeding regression turnaround time. In addition, a new channel recording and replay capability enables users to run entire regressions just once and perform playback later without stimulus generators for specific components of the verification environment.

"Synopsys and the EDA industry are seeing broad deployment of SystemVerilog," said Manoj Gandhi, senior vice president and general manager of the Verification Group at Synopsys. "We continue to provide technological leadership in this market with increased investments that address the growing verification challenges of our customers. The expanded release of VMM is the result of a successful and innovative collaboration between Synopsys, our customers and partners. It provides an excellent foundation for building a single, standardized verification methodology."

About VMM

The VMM methodology enables chip development teams to use SystemVerilog to create comprehensive verification environments using transaction-level, coverage-driven, constrained-random and assertion-based techniques, and specifies library building blocks for interoperable verification components. The latest enhancements to VMM are backward compatible with the previous version of VMM, compliant with SystemVerilog and entirely open source. The expanded release of VMM is available for immediate download at http://www.vmmcentral.org.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits of the new, expanded release of VMM. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section

of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and subsequent forms 10-Q, entitled "Risk Factors."

Editorial Contact:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900 x114
sbrennan@mcapr.com

SOURCE: Synopsys, Inc.

Web site: http://www.synopsys.com/
