Synopsys Adds Incremental Signoff-Quality Design Rule Checking to IC Compiler

Push-button flow and faster turnaround time speed up final stages of tapeout

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MOUNTAIN VIEW, Calif., Sept. 24 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the addition of incremental signoff-quality Design Rule Checking (DRC) and metal fill capability to IC Compiler. IC Compiler has accelerated hundreds of tapeouts across a broad range of technologies from 130-nm to 45-nm by providing correct-by-construction, DRC-clean layouts. As an added assurance, Synopsys is now rolling out new technology to guard against corner-case DRC violations that can remain unnoticed until the final stages of physical verification, critically impacting the tapeout schedule. The new push-button capability in IC Compiler is powered by Hercules DRC/LVS and enables place-and-route engineers to easily run physical verification after each block, ensuring that the final signoff verification will succeed in a single pass. Incremental capability allows users to run localized checks to verify layout modifications, reducing the turnaround time to minutes versus hours for full-chip verification.

"As we move into 65-nm and below, the number of foundry DRC checks during physical verification is growing significantly," said Keith Riley, vice president of Engineering at Intellon Corporation. "Being able to conduct DRC checking on routing layers incrementally using the foundry runset directly within IC Compiler allows us to verify quickly any possible layout modifications, such as manual Engineering Change Orders (ECOs). In early trials of the incremental capability, we have seen significant time savings in our design flow."

Intellon Corporation (NASDAQ: ITLN) is a leading provider of HomePlug-compatible integrated circuits (ICs) for home networking, networked entertainment, Ethernet-over-Coax (EoC) and smart grid applications. Intellon will integrate IC Compiler's signoff quality DRC checking into its production environment because of its ease-of-use and fast turnaround time. Traditionally, physical DRC checking has been a separate post-design step and not part of the physical implementation flow. In the case of a layout modification, designers need to go back, update the design database, validate the fixes against timing and other design goals, and then run full-chip DRC each time. By integrating DRC checking and metal fill into IC Compiler, Synopsys is enabling users to perform signoff-quality checks incrementally by calling Hercules from inside the implementation environment, where the impact of any changes on timing can be estimated.

"By adding incremental physical verification capabilities to IC Compiler, we are enabling users to save hours by eliminating unnecessary iterations during the final stages of the tapeout," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Running physical verification checks from within IC Compiler during the design process helps ensure that once implementation is done, final signoff will succeed in a single pass."

Incremental signoff DRC and metal fill are targeted for general production in the September, 2008 release of IC Compiler.

About IC Compiler

Synopsys' IC Compiler provides hand-craft-quality macro placement, intelligent power network support, and MinChip technology for automatic die-size reduction, all on a single timer foundation that enables faster time to closure with higher quality of results (QoR). For complex designs, a concurrent flow that seamlessly blends planning and implementation tasks and offers an integrated environment with a single timer and high correlation with sign-off is critical. Concurrent planning and implementation replaces the traditional "plan-then-implement" methodology, resulting in faster time to tapeout and reduced design cost.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits, availability, and performance characteristics of the addition of incremental signoff-quality Design Rule Checking and metal fill capability to IC Compiler. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties, uncertainties attendant to any new product release, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and subsequent forms 10-Q, entitled "Risk Factors."

SOURCE: Synopsys, Inc.

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