Synopsys Announces Availability of New Fully Synthesizable PowerPC Cores

New Cores Expand Configurability and Process Portability Choices

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MOUNTAIN VIEW, Calif., July 23 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the availability of fully synthesizable implementations of the IBM PowerPC® 460 and cache configurable PowerPC 405 embedded microprocessor cores as components of the DesignWare® Star IP program.

The PowerPC 460S is a 32-bit high performance, low-power embedded processor core optimized to meet the performance and power requirements of today's consumer electronics, communications, and storage applications. As a synthesizable version of IBM's PowerPC 464 hard core, the PowerPC 460S allows the system-on-chip (SoC) designer to select the L2 cache size, L1 cache size, and multi-core processor local bus necessary to optimize their design. Additionally, the PowerPC 460S supports an optional floating point unit.

The PowerPC 405S is a 32-bit low power, mid performance embedded processor core with design attributes that make it an ideal solution for emerging consumer, storage, wired and wireless applications. As a synthesizable version of IBM's most popular hard core series, the PowerPC 405S now supports a user-definable L1 cache size that helps SoC designers optimize performance and area to match the application requirements.

"These new synthesizable versions of the PowerPC 460S and 405S embedded cores take advantage of Synopsys' expertise in IP design, delivery and support to ease customers' integration effort," said Ron Soicher, vice president of Alliance Strategy, IBM Systems and Technology Group. "The combination of process portability and compatibility with standard synthesis-based design flows reduces major cost and design barriers, and make the Power Architecture more readily available to all SoC designers."

Developed through a close collaboration between IBM and the Synopsys Professional Services and DesignWare IP teams, the foundry-independent processor cores are supported by a broad range of design tools in the Synopsys Galaxy™ Design and Discovery™ Verification platforms. The PowerPC 460S and 405S processors are distributed as simulation and timing models and synthesizable register transfer level (RTL) cores. Synthesizable IBM CoreConnect™ peripherals are also available to licensees of the PowerPC cores. The combination of synthesizable PowerPC cores and CoreConnect peripherals with the DesignWare IP portfolio gives designers a comprehensive PowerPC solution spanning all facets of SoC design from system-level design to implementation.

"The addition of these new cores to our DesignWare Star IP portfolio highlights the success of our multi-year collaboration with IBM to deliver products that support the Power Architecture," said John Koeter, senior director for IP and Services at Synopsys, Inc. "These new cores offer designers a low-risk path to silicon with the flexibility to implement designs in their choice of process technologies."

Synopsys' distribution of the PowerPC cores supports the goals of Power.org™ by providing designers around the world with access to the Power Architecture and with a means to implement it in their preferred process technology. Power.org is an open organization that develops and promotes the Power Architecture™ and its supporting technologies. Synopsys is a founding member of Power.org.

Availability

PowerPC 460S and PowerPC 405S design views, including the simulation and timing models, a verification environment, and full documentation are currently available at no additional charge to DesignWare Library customers. For an additional fee, DesignWare Library users may license from IBM or Synopsys the implementation views of the core, including fully synthesizable RTL.

For more information, visit https://www.synopsys.com/designware-ip.html

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solution for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction level models to build virtual platforms for

rapid, pre- silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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