Synopsys Delivers Comprehensive Design Support for TSMC 40-Nanometer Process

TSMC and Synopsys Address Low Power and DFM Challenges with Reference Flow 9.0

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MOUNTAIN VIEW, Calif., June 4 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that it is delivering comprehensive support for TSMC Reference Flow 9.0 targeting 40-nanometer (nm) processes, including 40G and 40LP. Technologies that enable design readiness include: low power design and verification provided by the Eclypse™ Low Power Solution using the industry standard Unified Power Format (UPF); advanced Design-for-Test (DFT) capabilities; complete 40-nm design rule support for place-and-route; transparent half-node design flow; statistical leakage analysis; and enhanced design-for-manufacturing (DFM) capabilities. The two companies also extended the scope of their library distribution agreement to include TSMC's 45-nm and 40-nm Standard Cells, I/Os and Memory Compilers in Synopsys' DesignWare® Library product.

Low power design techniques provided in connection with Reference Flow 9.0 include multi-supply voltage, level shifter and isolation cells, power gating, IR analysis, low power clock tree synthesis, and static timing and leakage analysis. With the new reference flow, designers utilize UPF to specify consistent low power design techniques at all levels of their design flow. New DFT capabilities covered by Reference Flow 9.0 include power-aware ATPG, multi-mode scan insertion and the TetraMAX® N-Detect function to predictably achieve the highest test quality while reducing the cost of test. These technologies are available with the Galaxy™ Design Platform and Discovery™ Verification Platform.

Because tight integration between design and manufacturing is becoming increasingly important to achieve high yield, Synopsys is announcing enhanced support for TSMC Reference Flow 9.0, including improvements in both physical and electrical DFM capabilities for 40-nm readiness. For productivity gains during implementation, designers can use concurrent yield optimization for critical area reduction and hierarchical critical area analysis. Electrical DFM support has been improved to include table-based DFM-LPE extraction flow. In addition, PrimeYield LCC links to TSMC's enhanced Shape-to-Electrical (S2E) DFM engine, enabling contour-based extraction for timing and leakage simulation down to 40-nm. For faster turnaround time, PrimeYield LCC supports hierarchical LPC analysis. These enhancements in Reference Flow 9.0 identify additional manufacturing issues before tapeout, improving time-to-silicon and reducing potential delays due to redesign.

"Synopsys and TSMC have worked together to keep pace with the evolving challenges of deep submicron design," said ST Juang, senior director of Design Infrastructure Marketing at TSMC. "Synopsys' integration of UPF low power standards in Reference Flow 9.0 is just one example of the cutting-edge technology included in this flow."

"We've worked closely with TSMC to ensure that our design platforms, with advanced signoff analysis, DFM and low power technologies, offer the solutions that designers need to address complex, deep-submicron challenges," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "We look forward to a continued relationship with TSMC to address the challenges at 40- nanometer and below processes and offer our mutual customers a complete, low- risk solution from RTL to silicon."

About TSMC Reference Flow 9.0 Support

Reference Flow 9.0 accommodates comprehensive Synopsys-based RTL-to-GDSII using the Eclypse Low Power Solution with UPF support, the Galaxy Design Platform for RTL synthesis, physical implementation and signoff, and the Discovery Verification Platform with VCS®, HSPICE®, and HSIM™/Nanosim® for RTL verification and circuit simulation. As an integral part of the Reference Flow 9.0, Galaxy support includes:

- -- Design Compiler® and Design Compiler Graphical technology logic synthesis
- -- Power Compiler™ multi-voltage power management
- -- DesignWare Library and TSMC Nexsys Standard Cells and I/O libraries
- -- MVSIM and MVRC for voltage aware simulation and verification
- -- DFT MAX 1-pass test synthesis
- -- IC Compiler physical implementation, including low power clock tree synthesis (CTS)
- -- PrimeTime®, PrimeTime SI, PrimeTime Advanced on-chip variation

modeling (AOCVM), and PrimeTime VX static timing and signal integrity sign-off
-- PrimeRail power network sign-off
-- PrimeTime PX full-chip power and statistical leakage analysis
-- Star-RCXT™ extraction
-- Hercules™ PVS physical verification
-- TetraMAX automatic test pattern generation (ATPG)
-- PrimeYield LCC and PrimeYield CMP for design-for-yield analysis

Synopsys Professional Services is a global TSMC Design Center Alliance partner and provides expertise in chip implementation and flow deployment with Reference Flow 9.0. Synopsys also distributes TSMC libraries through the DesignWare Library.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to- silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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