Synopsys Donates Proven VMM Methodology Library and Applications to Accellera

Accellera Accepts Donation for Verification Standards Working Group

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MOUNTAIN VIEW, Calif., May 12 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that it is donating its complete implementation of the proven VMM verification methodology for SystemVerilog, including the VMM Standard Library and VMM Applications, to Accellera to enable verification interoperability standardization. Accellera has accepted the donation so the recently formed Accellera Verification IP (VIP) Technical Subcommittee can use it for their standardization activities.

The VMM methodology, originally defined in the Verification Methodology Manual for SystemVerilog, has been used successfully by hundreds of verification teams since its introduction in 2005. Synopsys' donation to Accellera addresses customers' demand for a modular, scalable and reusable design methodology standard while enabling them to more easily develop and share complex verification environments.

"Accellera's newest standardization activity will promote interoperability among vendors' and users' verification methodologies," said Shrenik Mehta, Accellera chair. "The donation of Synopsys' VMM implementation provides the technical subcommittee with established technology to meet their objectives."

"The enormous investment in the VMM methodology made by Synopsys, its partners and customers over the past four years has helped design teams around the world take full advantage of SystemVerilog," said Manoj Gandhi, senior vice president and general manager of the Verification Group at Synopsys. "Accellera's acceptance of Synopsys' donation of its complete implementation of the VMM methodology enables Accellera to leverage this investment to create a single, unified standard that will accelerate the pace of innovation."

Complete VMM Methodology

A complete methodology requires more than just a standard base class library. It requires applications that provide high-level functions to further increase productivity, macros and utilities to cut down testbench creation time, and clear documentation and examples to shorten the learning curve. Synopsys has donated its complete implementation of the VMM methodology, which includes:

* VMM Standard Library
* VMM Register Abstraction Layer application
* VMM Reusable Environment Composition application
* VMM Memory Allocation Manager application
* VMM Hardware Abstraction Layer application
* VMM Data Stream Scoreboard application
* VMM Macro Library

Trusted and Widely Used

Chip development teams need to have confidence that their verification methodology is mature, full-featured and scalable. One of the best ways to gain this confidence is to look for other teams who have used a methodology successfully on multiple projects. The VMM methodology has been successfully deployed by hundreds of project teams across the globe since 2005, and over 50 technical papers and tutorials on the VMM methodology have been presented at Synopsys User's Group (SNUG) meetings and other venues.

Broad Vendor Support

By way of the VMM Catalyst program, EDA suppliers throughout the industry are able to leverage VMM technology and expertise to create tools, verification IP (VIP), training, and services for chip development teams. More than thirty companies are currently members of the VMM Catalyst program.

VMM User Forum

Synopsys will be sponsoring a VMM luncheon at the Design Automation Conference (DAC) in Anaheim, Calif. on June 10, 2008. Join Synopsys and VMM users to explore how VMM has extended methodology beyond base classes. For more information and to register, please visit

https://www.synopsys.com/company/resources/synopsys-press.html . VMM will also be featured in Synopsys' main booth at DAC (booth # 1349) and in the Synopsys Standards Booth at DAC (booth # 1541).

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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