# Synopsys Releases Silicon Proven 5.0 Gbps PCI Express 2.0 PHY IP

New DesignWare PHY IP Provides Designers with Complete, Single Vendor IP Solution for the PCI Express 2.0 Interface

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MOUNTAIN VIEW, Calif., April 28 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the availability of the DesignWare PHY IP for PCI Express 2.0 (Gen II), based on the PCI Express 2.0 base specification. This product release further extends Synopsys' IP leadership by providing designers with the IP industry's only complete, silicon-proven PCI Express 2.0 IP solution, including digital controllers, PHY and verification IP from a single vendor. Accessing all the IP from one provider allows designers to lower the risk and cost of integrating the 5.0 Gbps PCI Express interface into their high performance system-on-chip (SoC) designs.

PCI Express 2.0 doubles the 1.1 specification transfer speed from 2.5 Gbps to 5.0 Gbps per lane, meeting the demand for both increased bandwidth and narrower interconnect links in data center, storage, high-end graphics and networking infrastructure applications. Backwards compatibility with the PCI Express 1.1 and PIPE specifications, allows designers to optimize performance and power while maintaining interoperability with existing devices. The DesignWare PHY IP substantially exceeds the PCI Express 2.0 electrical specification in areas such as jitter, margin and receive sensitivity, thus delivering a robust design without sacrificing performance. The DesignWare PHY IP for PCI Express 2.0 includes advanced built-in diagnostic capabilities and ATE test vectors enabling at-speed production testing of the PHY. It is implemented in standard CMOS digital technologies and does not require special process options, providing both ease of integration into a SoC, and ensuring high production yields.

"Synopsys continues to be an IP leader, by providing designers with a robust, silicon-proven PCI Express 2.0 PHY that supports the Common Platform technology," said David Steer, director of IP Business Development at Chartered Semiconductor. "By combining the DesignWare PHY IP with the multi-sourcing capabilities of Common Platform technology, designers benefit from having a high quality mixed-signal PHY that can be manufactured at multiple foundries using a single GDSII source."

"We have had an extensive relationship with Synopsys on PHY IP and have been very pleased with their architecture, technical knowledge, support and capability," said Regina Darmoni, director, Analog/Mixed Signal & Digital Foundry, IBM. "The DesignWare PHY for PCI Express 2.0, which is available in the 65-nm IBM ASIC offering and the 65-nm Common Platform foundry technology, enables us to successfully deliver high quality solutions to the market."

"PCI-SIG welcomes the introduction of the new Synopsys DesignWare PHY IP for PCI Express 2.0," said Al Yanes, PCI-SIG chairman and president. "As an active member of PCI-SIG, Synopsys helps to prepare the industry for the proliferation of the PCI Express technology and we are happy to see them enable designers to integrate the latest specification into their chips."

"With the release of the DesignWare PHY for PCI Express 2.0, designers can now get access to a complete silicon-proven IP solution from a single, trusted vendor," said John Koeter, senior director of marketing for IP and Services at Synopsys. "As the leading provider of PCI Express IP, we continue to invest heavily in our IP roadmap to deliver low risk, high quality IP solutions that help our customers bring differentiated products to the market faster."

Availability

The DesignWare PHY IP for PCI Express 2.0 is available in leading 65-nm foundry processes, notably the Common Platform technology from IBM and Chartered, which provides users with a unique "copy exact", multi-source capability enabling them to use multiple foundries with no design re-work.

The DesignWare IP digital controllers and verification IP for PCI Express 2.0 are also available today. For more information or to take a virtual tour of the Synopsys IP lab, please visit: http://www.synopsys.com/pciexpress. In addition, participate in the mixed-signal IP blog at: http://synopsysoc.org/msip-blog/

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for

system-on-chip designs. As the leading provider of connectivity IP, Synopsys delivers the industry's most complete solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.



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