Media Advisory/Alert: Synopsys Experts on the Road IP Seminar and Keynote Luncheon With Jeff Ravencraft, President of the USB-IF

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.
(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., Feb. 21 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, will host a free one-day IP seminar focused on low power IP including USB, DDR, PCI Express and embedded memory. At this seminar, learn how the latest low power features in the Synopsys DesignWare® IP portfolio can help lower cost and speed time-to-market for high-performance system-on-chip designs.

Attend a special luncheon keynote with one of the industry's expert authorities on the USB interface, Mr. Jeff Ravencraft, President of the USB Implementer's Forum.

TOPICS TO BE COVERED:

-- Understanding the Challenges of PCI Express Gen2 and Beyond
-- Decoding the Real Low Power Benefits of DDR3
-- Enabling Hi-Speed Chip-to-Chip Communications
-- Embedded Memory: Selecting the Optimal Memory Architecture

For more information or to register now, please visit:
http://www.synopsys.com/news/events/seminars/ip_seminar.html

WHAT: Experts on the Road IP Seminar

WHEN: March 5, 2008

WHERE: Santa Clara Hilton, 4949 Great America Parkway, Santa Clara, CA 95054

SEMINAR HOURS: 9:30 am to 3:15 pm

SESSION DESCRIPTIONS:

-- Understanding the Challenges of PCI Express Gen2 and Beyond
The PCI Express specification is evolving quickly in speed and functionality. Single Root and Multi-Root I/O Virtualization, Geneseo, Gen1, Gen2 and Gen3 are all things you will need to know if you are using PCI Express. This session covers the roadmap and how it applies to different market segments. We will also discuss the impact that the transition from 2.5Gbps to 5Gbps to 8Gbps and beyond has on the design of the PCI Express digital controller and PHY IP.

-- Decoding the Real Low Power Benefits of DDR3
DDR SDRAM interfaces have become increasingly difficult to design with data rates increasing by an average of 30 percent per year. This session highlights the low power benefits to the overall system when using DDR3 as compared to DDR2 SDRAMs. It will explore some of the issues encountered when migrating from DDR2 to DDR3 and conclude with an overview of the two distinct DesignWare DDR2/3 IP solutions.

-- Luncheon Keynote Jeff Ravencraft, President of USB-IF
Join Jeff Ravencraft, technology strategist with Intel and president of the USB Implementer's Forum, for an insightful discussion on the latest developments on the USB standard including Superspeed USB 3.0, High-Speed Inter-Chip Communication and Certified Wireless USB. Come see how these emerging standards can impact your chip designs.

-- Achieving Lower Power with USB Hi-Speed Inter-Chip Communication
Next generation USB-enabled mobile applications are requiring higher bandwidth and longer battery life. This session discusses the latest USB interface standards including High-Speed Inter-Chip (HSIC), which simplifies the connection down to two wires and eliminates the USB cable. Link Power Management (LPM) adds a new low power state that

enables faster suspend and resume times for traditional USB 2.0 applications. Learn more about the new Synopsys DesignWare USB IP products supporting these two standards.

-- Selecting the Optimal Embedded Memory Architecture
Today, designers are facing demands for increased performance and advanced features for SoC designs. The need for larger on-chip memories is becoming increasingly important to address performance bottlenecks, reduce system power consumption and cost. This session describes how to select the most optimal embedded memory architecture for your designs.

For more information on the Experts on the Road IP seminar, please visit: http://www.synopsys.com/news/events/seminars/ip_seminar.html

For more information on DesignWare IP, please visit: http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:
Yvette Huygen
Synopsys, Inc.
650-584-4547
yvetteh@synopsys.com

Ellen Van Etten
MCA, Inc.
970-778-6094
evanetten@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Yvette Huygen of Synopsys, Inc., +1-650-584-4547, yvetteh@synopsys.com; or Ellen Van Etten of MCA, Inc., +1-970-778-6094, evanetten@mcapr.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/