Synopsys' DesignWare DDR Protocol Controller IP Integrated Into Arteris' Network-On-Chip Interconnect Solution

Solution Enables High Bandwidth Data Transport Between SoC Subsystems and Off-Chip DDR Memory

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(NASDAQ:SNPS)

PARIS and MOUNTAIN VIEW, Calif., Jan. 30 /PRNewswire-FirstCall/ -- Arteris, the leading provider of Network-on-chip (NoC) solutions and Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the integration of Synopsys' DesignWare® DDR Protocol Controller IP and the Arteris NoC solution for complex system-on-chips (SoCs). This combination delivers reliable, high-speed, on-chip connectivity with low latency to external DDR2 and DDR3 SDRAM memory for advanced systems.

Applications such as digital TVs, set-top boxes, telecom and storage require high-performance data traffic between the various processor subsystems and on-chip peripherals that extend to off-chip DDR SDRAM memory. The integration of the silicon-proven DesignWare DDR Protocol Controller IP and the silicon-proven Arteris NoC solution addresses these challenges by providing designers with the necessary memory traffic bandwidth and quality of service.

"We have worked closely with Arteris to integrate the Synopsys DesignWare DDR Protocol Controller IP into the Arteris memory scheduler and NoC solution," said Joachim Kunkel, vice president and general manager of the Solutions Group at Synopsys. "Arteris' customers now have access to high-quality, pre-verified DDR Memory Controller subsystem IP, shortening design time and lowering risk."

The Arteris NoC is capable of operating at frequencies exceeding 750 MHz in a 65 nanometer (nm) process and offers link widths from 32 to 128 bits for high system bandwidth. The NoC typically uses fewer top-level wires compared to a traditional on-chip bus fabric. The highly configurable DesignWare DDR Protocol Controller IP supports the latest DDR2 and DDR3 memory devices operating at up to 1600 Mbps. Synopsys provides a complete, silicon-proven IP solution comprised of a digital controller core, mixed-signal PHYs targeting today's leading foundries and process nodes, and verification IP for subsystem and system-level verification.

"The Arteris NoC and Synopsys DesignWare DDR Protocol Controller IP solution allows designers to quickly create highly complex SoCs in deep submicron technologies, while saving significant internal development costs," said K. Charles Janac, president and chief executive officer of Arteris. "Synopsys' technology leadership in the DDR IP and connectivity IP markets makes them an ideal partner for our advanced NoC products."

Availability

The Arteris NoC IP solution and the integration kit for the Synopsys DesignWare DDR Protocol Controller IP are available from Arteris immediately.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express®, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-

to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/

About Arteris

Arteris, Inc. provides Network-on-Chip (NoC) IP and associated design tools to improve the performance of system-on-chip (SoC) architectures for multimedia, telecom, and mobile applications. Arteris' NoC solution manages the on-chip communications within complex SoCs delivering high performance, while reducing the number of global wires and lowering power consumption. It allows chip developers to implement efficient and high-performance SoC designs, overcoming limitations of traditional layered or pipelined bus-based architectures. Arteris' technology is scaleable in terms of the number of IP blocks designers can network, as well as with deep submicron silicon manufacturing processes. The Arteris NoC solution is compatible with existing design flows and IP interface standards.

Arteris operates globally with headquarters in San Jose, California and an engineering center in Paris, France. Arteris has raised more than $24 million in equity funding from an international set of investors. More information can be found at http://www.arteris.com/.

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