Synopsys Recognizes Engineers' Technical Excellence With Best Paper Awards at 16th Annual SNUG Europe Conference

Popularity and Longevity of Conference Showcases User and Contributor Commitment to Solid Technical Content

Munich, Germany
SNPS

MUNICH, GERMANY – October 23, 2007 - Synopsys, Inc. (Nasdaq:SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the Best Paper Awards for the 16th annual Synopsys Users' Group (SNUG®) in Munich, Germany. At the Munich event, the first place award for Best Paper went to Kees Timmermans and Simon Meintema ofTTA-International for "Automated Development of Schematic Documentation for Web-Delivery." Second place went to Dan Steinberg of Integrated Device Technology for "Regression & Random Sims: Techniques & Recommendations." Third place went to Jacob Andersen, Peter Jensen and Stig Kofoed of SyoSil for "Standardizing Verification IP Reuse by Introducing SystemVerilog Verification Components."The award for Best First-Time Presenter went toJuergen Dirks of LSI Corporation for "Mix and Match of Flat, Hierarchical and Pseudo-Hierarchical Approaches for Different Steps of a Design Flow."The winning papers were selected by the attendees and the SNUG Technical Committee.

The Technical Committee Award went toRoberto Mattiuzzo and Saverio Graniello of STMicroelectronics and Salvatore Talluto, Alfredo Conte and Adam Cron of Synopsys, Inc. for "Small Delay Defect Testing." Two Technical Committee Honorable Mentions went to David Sebastio of Texas Instruments Inc. and a co-author for "Analog Simulations of High-Speed Serial Chip-to-Chip Links with HSPICE®," and to Stuart Vernon of Imagination Technologies Ltd. and Simon Bloyce of Synopsys, Inc. for "Easing the Pain of Sign-off Timing and SI Closure Using PrimeTime® Distributed Multi-Scenario Analysis."

SNUG Europe is part of a global program that last year drew more than 5,000 integrated circuit (IC) and system design engineers to 10 such technical conferences worldwide. The flagship event in San Jose, California drew record attendance of nearly 1,600 Synopsys users in March of 2007. Attendees represent the world's largest semiconductor design and manufacturing companies as well as many innovative start-ups.

“Year after year, we get positive feedback from users about the quality and breadth of SNUG’s technical content,” said Frank Poppen, research engineerat OFFIS Institute for Information Technology and SNUG Europe technical chair. “Users from all over Europe gather to network and exchange ideas about the technical challenges in semiconductor design and manufacturing. SNUG gives them broad exposure to a range of hot topics in the industry, particularly those unique to European markets and applications.”

Aart de Geus, chairman and chief executive officer at Synopsys, addressed attendees at the technical conference with a keynote that focused on what Synopsys is doing to help customers with their challenges in achieving higher quality of results (QoR), faster time to results (TtR) and lower cost of results (CoR). He gave an industry overview that set the context for the economic and technological challenges in the industry and then took a deeper look into QoR, specifically focusing on power management challenges and solutions from system level to manufacturing. He also highlighted some of the exciting progress Synopsys has made in the past year in the TtR arena with advanced verification solutions and IP, and CoR progress with improved yield technology.

“SNUG is a great opportunity for our customers to exchange ideas and give Synopsys executives honest feedback on what we’re doing right and where we can improve,” said Mr. de Geus. “The open communication and vibrant collaboration at SNUG conferences make them premier technical events in the EDA industry. This year’s best paper winners exemplify that cooperative spirit and we thank them for sharing their technical insights.”

SNUG Europe Sponsors include: Global Sponsors ARM and TSMC; Gold Sponsors Hewlett-Packard and Virage Logic, and Common Platform Technology members Chartered Semiconductor, IBM and Samsung. The two-day SNUG Europe conference featured a technical program with more than 70 presentations that focused on all areas of design including synthesis, verification, low-power design, physical design, test and design-for-manufacturing. This year’s program featured 49 user papers, 26 Synopsys technical tutorials and two panels. These presentations focused on the challenges that engineers face as they design complex systems for a wide

array of applications. Unique to SNUG Europe is the multi-technology systems track, geared towards users in the automotive, aerospace and IC industries. Conference proceedings are available on the SNUG website: http://snug-universal.org/

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com.

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