# Synopsys Customers Accelerate Yield Learning With Converged Test and Yield Management Data Flow

New Odyssey DFT Module Connects TetraMAX Diagnostics with Odyssey Yield Management to Enable Comprehensive Failure Analysis of Production ICs

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.
(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., Oct. 23 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced general availability of the Odyssey Design-for-Test (DFT) module for use by design organizations worldwide. The Odyssey yield management software has been widely adopted by leading semiconductor manufacturers to correlate and analyze diverse datasets needed for product yield enhancement. The TetraMAX® automatic test pattern generation (ATPG) solution creates high-quality manufacturing tests and identifies logic in a design that could contribute to observed tester failures. TetraMAX failure diagnostics data is exported to the new Odyssey DFT module to facilitate comprehensive failure analysis and rapid yield improvement of fabricated devices. Fabless firms have adopted the Synopsys solution because shorter yield-learning cycles can increase net profits over a product's life cycle. Synopsys will demonstrate the yield enhancement suite at this year's International Test Conference (ITC) in Santa Clara, Calif., October 23-25 (booth #212).

"If a device fails production test, we want to understand why," said Bruce Cory, DFT manager at NVIDIA Corporation. "The Synopsys yield management solution allows us to leverage design, fabrication, and production test data to analyze TetraMAX diagnostic isolations across multiple die and wafers. The software helps identify underlying failure signatures to enable faster yield ramp."

Semiconductor foundries typically supply their fabless clientele with parametric data associated with the manufacture and testing of production parts, but until now there was little designers could do with the information to improve product yield. With the Synopsys tools in-hand, designers are now leveraging the foundry-supplied data together with failure diagnostics accumulated from production runs (a capability often referred to as "volume diagnostics") to help determine the root cause of yield loss.

For example, designers at NVIDIA Corporation and TranSwitch Corporation are using the Odyssey solution to correlate circuit failure candidates reported by TetraMAX diagnostics with foundry-supplied information. Data mining and cross-correlation features in Odyssey assist designers in quickly determining both the impact of measured process parameters on product yield and whether failing parts are caused by systematic or random processes.

"Nanometer manufacturing steps can distort device and wire geometries, leading to more frequent failures at process corners," said Zahi Abuhamdeh, director of DFT and Diagnostics at TranSwitch Corporation. "Also, the foundry's occasional tweaking of the process can cause subtle corner failures that previously did not occur. The Synopsys yield enhancement solution has provided us the ability to determine whether failing parts from a product run are due to foundry, specification, or design-specific issues. In the latter scenario, making alterations to a single library cell or including or removing a foundry-recommended design rule might lead to a step-increase in the product's yield."

"Synopsys is committed to providing both foundries and their fabless clientele the latest innovations in ATPG diagnostics and yield management systems," said Dr. J. Tracy Weed, director of the Manufacturing Products Group at Synopsys. "With the Odyssey DFT module, our customers now have vastly improved automation that enables analysis of product-specific diagnostics, design and foundry-supplied data to identify yield delimiters that present a barrier to higher profitability."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, sgulizia@synopsys.com; or Lisa Gillette-Martin of MCA, Inc., +1-650-968-8900, ext. 115, lgmartin@mcapr.com

Web site: http://www.synopsys.com/