Synopsys NanoTime Improves Timing Verification on NetLogic Microsystems 65-Nanometer Processor

NanoTime Enables Greater Than 3X Improvement in Timing Verification Performance for NetLogic Microsystems

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MOUNTAIN VIEW, Calif., July 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that NetLogic Microsystems, Inc. has taped out its next-generation knowledge-based processor using Synopsys' NanoTime transistor-level static timing analysis (STA) solution. This 65-nanometer processor was optimized for high-performance packet processing and low power consumption. NanoTime played a critical role in improving timing verification performance by more than 3X while maintaining 5 percent silicon accuracy.

"As the leader in knowledge-based processors, we required a comprehensive static timing solution that addressed both gate- and transistor-level blocks to help us improve the development timeline and quality of results of our full-chip designs," said Dimitrios Dimitrelis, vice president of Engineering at NetLogic Microsystems. "NanoTime integrates seamlessly with the Synopsys PrimeTime suite, resulting in a comprehensive solution that enabled us to achieve a 3X performance improvement while maintaining 5 percent silicon accuracy."

NanoTime offers designers higher predictability and improved productivity over existing transistor-level solutions. Its concurrent timing and signal integrity (SI) features enable designers to accurately and quickly identify timing issues early to avoid expensive silicon respins. With its superior ability to recognize complex custom design structures and its embedded dynamic circuit simulation technology, NanoTime helps ensure silicon-accurate analysis. NanoTime delivers the performance and capacity required to perform analysis of complex circuits. Designers' productivity is further boosted by significant ease-of-use features, including interactive STA, extracted timing model (ETM) creation, and seamless integration with Synopsys' PrimeTime® full-chip STA solution.

"Many customers, such as NetLogic Microsystems, continue to require custom digital design techniques to meet the high-performance demands of their increasingly complex applications," said Ahsan Bootehsaz, vice president of Research and Development, Synopsys Implementation Group. "Synopsys provides this customer base with a unique analysis solution. NanoTime not only delivers the productivity of static timing analysis to transistor-level design, but its seamless integration with Synopsys' PrimeTime suite, the industry's gold-standard for timing verification, enables a full-chip sign-off solution."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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