Synopsys Launches VMM Catalyst Program With More Than 50 Member Companies

Program Accelerates Development of VMM-Enabled Verification Tools, IP, Services and Training

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MOUNTAIN VIEW, Calif., June 5 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced its VMM Catalyst Program to further accelerate widespread adoption and support of the industry-leading VMM verification methodology for SystemVerilog. Focusing on the methodology described in the Verification Methodology Manual (VMM) for SystemVerilog book, the VMM Catalyst Program is open to electronic design automation (EDA) vendors, silicon and verification intellectual property (IP) companies, and training and service providers to benefit mutual customers by advancing tool interoperability and the availability of IP and services using the VMM methodology. Industry support from more than 50 firms and widespread customer adoption has established the VMM methodology as the de facto standard methodology for verifying complex electronic chips.

The VMM Catalyst program helps meet the growing demand for productive and interoperable verification flows taking advantage of the full power of SystemVerilog. VMM-enabled EDA tools allow users to work at higher levels of abstraction, thereby increasing productivity. Verification IP created according to the VMM methodology allows for easy "plug-and-play" use in VMM testbenches. Verification consultants with VMM expertise can quickly create or enhance their client's verification environment, without having to spend time learning or developing a non-standard methodology. Training companies can help verification teams rapidly adopt the best practices incorporated in the VMM methodology. Engineers will therefore be able to choose from an even wider array of VMM-enabled offerings to speed development and deployment of verification environments.

Corporate members of the VMM Catalyst Program can gain access to Synopsys VMM-enabled products such as VCS®, Pioneer-NTB, the VCS Verification Library of bus protocol verification IP, and the SystemVerilog source code for the VMM Standard Library. This access enables the development and support of corporate members' respective VMM-enabled tools, IP, training and services. By providing these tools, verification IP and source code, Synopsys is accelerating the adoption of a complete and consistent methodology usage across all VMM Catalyst Program member companies. VMM Catalyst program members meeting certain requirements may also use Synopsys' "VMM-enabled" logo with their products or services to indicate interoperability with or support of the methodology.

"The VMM is the industry-leading methodology for SystemVerilog. It is being used by hundreds of design teams around the world and is supported by Synopsys' full range of VMM-enabled tools, verification IP, services and training," said George Zafiropoulos, vice president of marketing, Discovery Verification Platform at Synopsys, Inc. "We welcome the VMM Catalyst program members and look forward to their contributions to the growing VMM methodology ecosystem."

"The VMM methodology is a vital addition to the infrastructure needed to support the adoption of SystemVerilog. VMM provides both the building blocks necessary for rapid adoption of the language and the framework for a standard methodology," said Scott Sandler, CEO of Novas. "At Novas, we've responded to growing customer demand to make our Verdi™ Automated Debug System VMM-enabled -- qualifying our compilers against VMM-based descriptions, providing advanced visualization of class

structures and dynamic data, and ensuring that our current and future SystemVerilog Testbench capability delivers maximum benefit for VMM users."

"The Synopsys VMM Catalyst Program provides an effective forum for multiple vendors to offer compatible and interoperable verification solutions," said Lauro Rizzatti, general manager of EVE USA. "EVE has worked closely with Synopsys to support the VMM Hardware Abstraction Layer with the ZeBu platform, enabling a single SystemVerilog Testbench to easily target either ZeBu or VCS."

"The VMM methodology's growing popularity affirms the need for robust infrastructure solutions, and Synopsys' VMM Catalyst program will help enable even more innovation in this area," said Sashi Obilisetty, CEO of VeriEZ Solutions. "Our VMM-enabled EZVerify productivity solution for SystemVerilog provides over 50 built-in checks for VMM rules, guidelines and suggestions to help speed methodology adoption and creation of interoperable, reusable verification components."

"Paradigm Works is at the forefront of deploying advanced methodologies for the functional verification of complex ICs," said Michael Hoyt, CEO of Paradigm Works. "The VMM methodology details proven verification practices engineers can leverage when using SystemVerilog, and the introduction of the VMM Catalyst program will further accelerate the rate of VMM adoption. Already today, half of Paradigm Works' clients, including leading systems and semiconductor customers worldwide, are using the VMM methodology."

"As active collaborators over many years with both Synopsys and ARM we've been engaged with the VMM methodology from early on," said Rob Hurley, CEO of Doulos. "The Synopsys VMM Catalyst program enables the growing VMM user base to access high-capability training and support from partners such as Doulos. We're pleased to offer our two-day VMM Adopter Workshop to help the expanding number of VMM users get SystemVerilog out of the box to improve verification results and efficiency."

Founding members of the VMM Catalyst program include: Ammos Software Technologies, ARM, Avery Design Systems, Blue Pearl Software, Bluespec, Calypto Design Systems, Certess, Computer Based Education, Contemporary Verification Consultants, Denali, Doulos, eInfochips, Esterel Technologies, EVE, Fortelink, HCL Technologies, Ingot Systems, IntelliProp, Interra Systems, Intrinsix, IPextreme, JEDA Technologies, Kacper Technologies, Masamb Electronics Systems, MindTree Consulting, NoBug, Novas Software, nSys Design Systems, Patni Computer Systems, Paradigm Works, Productivity Design Tools, Perfectus Technology, Rainbow Cyclone, Real Intent, Silicomotive Solutions, Silicon Interfaces, SONAC, Sunburst Design, Sutherland HDL, Synplicity, TES Electronic Solutions, TrustIC, TransEDA, TooMuch Semiconductor, UV-Tech Consulting & Training, VeriEZ Solutions, Verific Design Automation, Verification Central, Verilab, VeriSure Consulting, Willamette HDL, Wipro Technologies, XtremeEDA, and Zocalo Tech.

Additional Information

For more information about the VMM Catalyst Program, visit
https://www.synopsys.com/community/interoperability-programs.html

About VMM Methodology

The VMM verification methodology for SystemVerilog is the industry-leading, de facto standard for architecting robust, powerful and productive verification environments for complex electronic systems, systems-on-chips (SoCs) and IP. The VMM methodology is defined in the Verification Methodology Manual (VMM) for SystemVerilog, published by Springer. The manual, co-authored by verification experts from ARM and Synopsys, describes how to use SystemVerilog to create comprehensive verification

environments using coverage-driven, constrained-random and assertion-based techniques, and specifies library building blocks for creating interoperable verification components. More information is available at http://www.vmm-sv.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA
650-968-8900 x114
sbrennan@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, sgulizia@synopsys.com; or Stephen Brennan of MCA, +1-650-968-8900 x114, sbrennan@mcapr.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/
