Synopsys Announces the Industry's First Comprehensive SATA AHCI IP Solution

Solution Reduces Integration Effort with Standard Software and Hardware Interfaces

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MOUNTAIN VIEW, Calif., May 30 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the release of the Synopsys DesignWare® Serial ATA (SATA) Advanced Host Controller Interface (AHCI) solution. With this addition to its DesignWare library, Synopsys becomes the industry's first intellectual property (IP) provider to offer all the required elements of a SATA AHCI interface including the SATA AHCI Digital Host Controller, SATA PHY and SATA Verification IP (VIP). The AHCI specification describes the register-level interface for a host controller, providing a standardized hardware and software interface that, results in reduced integration effort. Building on Synopsys' proven expertise in delivering IP solutions, this comprehensive SATA solution provides a low risk, easy-to-integrate solution that enables designers developing SATA AHCI-compliant systems to quickly implement a full-featured SATA host interface with native AHCI in their designs.

The DesignWare SATA AHCI core is compliant with the SATA 2.6 specification and AHCI 1.1 specification, and includes an ARM® AMBA® 2-compliant subsystem interface. With the industry-standard software and hardware interfaces, designers can reduce the time required to integrate the core into their design. The DesignWare SATA AHCI core has been verified against the industry-standard AHCI software drivers provided as part of the Linux® and Windows Vista™ operating systems. The AHCI standard programming interface reduces custom platform software driver creation, which in turn reduces the overall time from prototype to production. To meet the needs of low-power device operation, the DesignWare core includes aggressive power management strategies that enable the core to both initiate power-down modes and allow clocks to be turned off in these modes, resulting in very-low power consumption. The integrated Direct Memory Access (DMA) and configurable multiple independent SATA ports help ensure high performance operation on both the SATA interface and the system bus interface.

The core is delivered with DesignWare Verification IP and includes a subset of directed and constrained random tests to verify that the user-defined configuration functions correctly. The designer can leverage these tests and Verification IP to jumpstart the subsystem and system-level application-specific verification. The DesignWare SATA AHCI controller and the DesignWare SATA PHY constitute a seamlessly integrated, pre-verified SATA AHCI-compliant solution that accelerates time-to-market and reduces risk. In addition, the DesignWare SATA AHCI controller includes a highly configurable PHY link layer which has been proven to be interoperable with many third-party SATA PHYs.

"It's important for companies like Synopsys to show continued support for advancing the SATA technology," said Conrad Maxwell, SATA-IO marketing chair. "IP solutions like the new DesignWare SATA AHCI core demonstrate Synopsys' commitment to providing solutions that enable designers to implement and bring products to market quickly."

"The SATA AHCI solution enables designers to improve system performance through integrated DMA, reduce power through advanced power management techniques, and use Linux and Vista drivers, out-of-the-box," said John Koeter, senior director of marketing, IP and Services at Synopsys. "By utilizing Synopsys' SATA AHCI solutions, customers can accelerate time-to-market, reduce the risk associated with implementing the protocol and achieve better productivity."

Availability

The DesignWare SATA AHCI core, SATA PHYs and Verification IP are available now. For more information, visit: https://www.synopsys.com/designware-ip/interface-ip/sata.html .

Synopsys DesignWare IP solution for the SATA AHCI protocol also offers an optional automation tool, coreAssembler, for assembling and configuring the IP in the context of a complete subsystem. For more information, visit: https://www.synopsys.com/dw/ipdir.php?ds=core_assembler .

About DesignWare Cores

Synopsys DesignWare Cores provide system designers with silicon-proven, digital, and mixed-signal connectivity IP for some of the world's most recognized products, including communications processors,

routers, switches, game consoles, digital cameras, computers and computer peripherals. Provided as synthesizable RTL source code or in GDS format, these cores enable designers to create innovative, cost-effective system-on-chips and embedded systems. Synopsys provides flexible licensing options for the DesignWare Cores. Each core can be licensed individually, on a fee-per-project basis, or users can opt to license all the cores as part of one simple agreement. For more information on DesignWare IP, visit: http://www.designware.com/.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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