Synopsys and ARM Optimize Reference Methodology for Aggressive Power Management

Enhanced Flow Uses Synopsys' IC Compiler and DC Topographical Technology to Manage Leakage for 65-Nanometer and Below Processes

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MOUNTAIN VIEW, Calif. and CAMBRIDGE, England, May 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software and ARM (LSE: ARM); (NASDAQ: ARMHY), today announced an enhanced implementation Reference Methodology (iRM) for the ARM1176JZF-S™ synthesizable microprocessor that supports a wide array of aggressive power-management techniques. These silicon-proven best practices, delivered as scripts and documentation, enable the rapid implementation of the ARM1176JZF-S processor with both high application performance and low leakage power during standby operation. These practices are documented in the "Low Power Methodology Manual," published by Springer Science+Business Media [also announced today: 'New low power methodology manual demystifies advanced power management']. The enhanced iRM uses the Synopsys Galaxy™ Design Platform, including IC Compiler and Design Compiler® topographical technology, to harness these advanced power-management techniques and provide a comprehensive implementation solution that reduces risk and enables predictable success. The enhanced flow provides engineers with the latest in aggressive power-management technology.

The ARM1176JZF-S high-performance applications processor is widely used in a broad range of market segments, including networking, entertainment, consumer, imaging and wireless. The low-power design is enhanced with support for ARM's Intelligent Energy Manager™ (IEM) technology and various low-power modes. These low-power modes allow full use to be made of the leakage mitigation techniques supported in the enhanced iRM, including MTCMOS power gating with state retention as well as multi-threshold voltage optimization. Combined with the enhanced iRM, IEM enables dynamic power-reduction techniques such as dynamic voltage and frequency scaling with multi-corner, multi-mode optimization.

"As a licensee of ARM's microprocessors, we utilize the ARM-Synopsys Reference Methodology (RM) to enable quick time to market for our customers' SoC devices," said Alan Aronoff, vice president of marketing and business development for the fabless ASIC company Key ASIC, Inc. "As a developer of SoCs for consumer and portable applications, we are pleased to see the RM evolve to support differentiating SoC features we use such as optimizing power dissipation and intelligent power management."

The iRM can be ported to any process and standard cell library with the required low-power library components. It has been developed with ARM Advantage™ memories and standard cell libraries, including the Power Management Kit (PMK), part of ARM's family of Artisan® physical IP, which provides a comprehensive collection of low-power library cells.

"This methodology was developed as part of the ongoing ARM and Synopsys Technology Partnership," said Graham Budd, general manager, Processor Division, ARM. "The initial phase of the project delivered a comprehensive technology demonstrator including fully functional silicon, boards, operating system and application code. This project evaluated a wide variety of different leakage mitigation techniques and the best practices from this research were captured in the updated iRM for the ARM1176JZF-S processor. This iRM enables our customers to easily implement the most effective power-reduction techniques using the ARM1176JZF-S processor and Synopsys solutions in the process technology of their choice."

ARM and Synopsys will share the results of their low-power collaboration through a series of events at the Design Automation Conference (DAC) to be held in San Diego, CA, June 4 - 8, 2007. Events include a Low-Power Lunch (Convention Center, Room #28 ABCDE, 11:30AM), daily Synopsys Demonstration Suites case study sessions on low power implementation of an ARM1176JZF-S processor (Register at: http://eventreg.synopsys.com/dac/external/jsp/Login.jsp), and sessions at the "Tech Expert Theater" at the Synopsys Booth #5278, as well as the aggressive leakage management silicon technology demonstrator in the Synopsys Partner Booth #5273.

"We knew that undertaking a project like this meant collaborating on the early science, aligning product development roadmaps and integrating the individual low-power products from both companies into a single deployable solution," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "By building real silicon-based systems, we are well-positioned to understand and address the challenges faced by our mutual customers in their efforts to build low-power products and get them to market quickly. The collaboration results that serve as the basis for this RM enable designers to quickly

employ aggressive power-management techniques for the ARM1176JZF-S processor are also captured in the 'Low Power Methodology Manual.'"

Availability

The enhanced implementation Reference Methodology, which is based on the Synopsys Galaxy 2007.03 release, will be available to ARM1176JZF-S processor licensees from ARM in Q3 of 2007. The ARM1176JZF-S processor, supporting power gating and IEM, is available today.

About ARM

ARM designs the technology that lies at the heart of advanced digital products, from mobile, home and enterprise solutions to embedded and emerging applications. ARM's comprehensive product offering includes 16/32-bit RISC microprocessors, data engines, graphics processors, digital libraries, embedded memories, peripherals, software and development tools, as well as analog functions and high-speed connectivity products. Combined with the company's broad Partner community, they provide a total system solution that offers a fast, reliable path to market for leading electronics companies. More information on ARM is available at http://www.arm.com/.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chip (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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