Synopsys Unveils Industry's First Certified Hi-Speed USB 'On-the-Go' nanoPHY IP for TSMC'S 65-Nanometer Process

Silicon-Proven DesignWare USB 2.0 nanoPHY Enables Designers to Reduce Risk and Speed Time-to-Market

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MOUNTAIN VIEW, Calif., May 15 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that its DesignWare® USB 2.0 nanoPHY is the first USB 2.0 PHY intellectual property (IP) for TSMC's 65-nanometer (nm) process to successfully pass the USB Implementers Forum Hi-Speed On-The-Go (OTG) PHY certification. Synopsys' industry-leading USB 2.0 nanoPHY mixed-signal IP, now available in the TSMC 65-nm process nodes, uses half the power and die area compared to previous USB solutions and enables faster time-to-market and reduced risk.

In addition to optimizing for low power and area, Synopsys IP architects designed the DesignWare USB 2.0 nanoPHY for long-term electrical performance of the USB 2.0 nanoPHY when implemented in the 2.5 V transistor process option. Since the nanoPHY must maintain USB compliance and thereby support 3.3V and 5V signaling levels, careful attention was required to ensure that the 2.5V structures would not be overstressed. Extensive simulations were specifically developed across worst-case conditions to ensure consistent, long-term nanoPHY operation.

The DesignWare USB 2.0 nanoPHY is part of the complete USB OTG solution from Synopsys. Combined with Synopsys' USB 2.0 high-speed OTG controller and USB Verification IP, Synopsys offers a proven, 65-nm solution for high speed OTG applications. The DesignWare USB IP products, including the PHYs have been certified in hundreds of applications.

"Designers require that we provide them access to reliable, low-risk and proven mixed-signal connectivity IP such as USB 2.0," said Kuo Wu, deputy director of design service marketing at TSMC. "This latest generation of USB 2.0 nanoPHYs from Synopsys allows designers to quickly integrate USB 2.0 connectivity into their system-on-chip designs and ramp into high-volume production."

Synopsys' USB 2.0 nanoPHYs are available for TSMC's 65-nm, 90-nm, and 130-nm processes.

"The availability of proven mixed-signal IP continues to be a key factor in enabling migration of SoC designs to advanced small-geometry processes," said John Koeter, senior director of IP Marketing at Synopsys. "We've worked closely with TSMC in creating this 65-nm USB 2.0 nanoPHY IP to help designers achieve power and area savings while meeting TSMC's rigorous design-for- manufacturing standards. Our attention to these details provides designers the confidence that the nanoPHY will deliver low power, small area, maximum yield and long-term reliability."

Availability

Synopsys' DesignWare USB 2.0 nanoPHY IP is available now from Synopsys for TSMC's 65-nm, TSMC's 90-nm, and TSMC's 130-nm processes.

About DesignWare Mixed-Signal IP

Synopsys enables designers to quickly integrate analog Mixed-Signal IP (MSIP) into next-generation system-on-chips (SoCs) with a comprehensive portfolio of high-performance PHYs for the PCI Express, SATA, XAUI, and USB protocols. The MSIP offering also includes a complete suite of I/O Libraries. Available for industry-leading processes, DesignWare Mixed-Signal IP meets the needs of today's high-speed designs for the networking, storage, computing, and consumer electronics markets. The DesignWare MSIP offering is complemented by a comprehensive suite of digital controller cores and verification IP to provide chip developers with a complete solution for SoC integration. Each MSIP can be licensed individually, on a fee-per-project basis or customers can opt for the Volume Purchase Agreement, which enables them to license all the MSIP in one simple agreement. For more information on DesignWare MSIP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-

market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

SOURCE: Synopsys, Inc.

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