Leading Semiconductor Companies in China Adopt the VMM Verification Methodology

Chinese-Language Edition of the Verification Methodology Manual (VMM) for SystemVerilog to Be Published by Beihang Press

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MOUNTAIN VIEW, Calif. and BEIJING, May 14 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the VMM verification methodology, described in the ARM-Synopsys Verification Methodology Manual (VMM) for SystemVerilog, has been adopted by major electronics companies in China for developing advanced verification environments. In addition, Synopsys announced that the Chinese- language edition of the manual has been published by Beihang Press in China. More than 3,500 copies of the English-language edition have been sold to date.

The manual, co-authored by verification experts from ARM and Synopsys, describes how to use SystemVerilog to create comprehensive verification environments using coverage-driven, constrained-random and assertion-based techniques, and specifies library building blocks for interoperable verification components. The VMM methodology is used by hundreds of system-on- chip (SoC) and silicon intellectual property (IP) verification teams around the world to speed development of powerful SystemVerilog-based verification environments and to help achieve measurable functional coverage goals in less time with less effort.

"Mainstream chip design increasingly requires the use of SoC-based design techniques with extensive IP reuse. This increased level of design complexity presents engineers with even greater verification challenges that require the adoption of powerful new verification techniques and methodologies," said Ji Jin, vice president of research and development at Spreadtrum. "We have applied the VMM methodology in our design flow, which has significantly improved the quality and productivity of our chip verification process. The VMM for SystemVerilog is an important and practical reference book for chip designers and verification engineers."

"A robust, systematic and predictable verification methodology is a necessary foundation for developing complex SoC products," said Xu Lei, chief technical officer of Tongfang Microelectronics Company. "The VMM methodology embodies industry best practices for developing and using advanced verification techniques with SystemVerilog. The VMM for SystemVerilog will help readers master the most advanced verification methods, no matter if they are verification engineers, design engineers or project directors."

"Verification of chips has become a challenge to engineers as design size and complexity increase. SystemVerilog with the VMM methodology can help chip developers solve the verification challenge effectively," said Dr. Liu Weiping, chief executive officer of CEC Huada Electronic Design. "Synopsys and ARM are to be applauded for introducing SystemVerilog-based verification techniques to China with the publication of the VMM for SystemVerilog. Chip development teams in China adopting the VMM methodology can now easily benefit from the advanced design verification methods used by experts worldwide."

"The widespread adoption of SystemVerilog in China is enabling a new generation of chip developers to take advantage of advanced verification techniques for complex SoC designs," said Dr. Tan Jun, president of ARM China. "The VMM for SystemVerilog, co-written by ARM and Synopsys, is an excellent guide for harnessing the power of SystemVerilog to improve verification productivity and quality."

"The VMM verification methodology has rapidly emerged as the de facto industry standard for SystemVerilog, enabling chip development teams around the world to achieve predictable verification success" said George Zafiropoulos, vice president of marketing, Discovery Verification Platform at Synopsys. "The publication of the Chinese-language edition of the Verification Methodology Manual for SystemVerilog represents a major step in bringing these advances to the growing community of chip developers in China."

A free technical tutorial on the VMM methodology, and Synopsys' recently introduced VMM Applications for rapid verification environment development, will be delivered at the Synopsys Discovery Verification Seminars in Beijing, China on May 14, 2007; Shanghai, China on May 16; and Shenzhen, China on May 17. More information is available at http://www.synopsys.com/news/events/seminars/veri_sem.html.

Availability

The Chinese-language edition of the VMM for SystemVerilog is available now from Beihang Press at RMB58 in major bookstores throughout China. For additional information, please visit: http://www.vmm-sv.com/.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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