Synopsys Design Compiler Topographical Technology Adopted by IBM to Accelerate ASIC Designs for Customers

5% Correlation Between Synthesis and Layout Key to Predictable ASIC Design Flow

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MOUNTAIN VIEW, Calif., May 7 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that IBM has added support for topographical technology in its 90- nanometer (nm) and 65nm-based application-specific integrated circuit (ASIC) design kits. Synopsys' Design Compiler® topographical technology enables IBM's ASIC customers to achieve tighter correlation between design results such as timing and power seen during synthesis and the results achieved after layout. This eliminates the need for time-consuming iterations between synthesis and layout to achieve design closure, thus significantly accelerating overall design time.

"We are pleased with the results we have seen with topographical technology. During our evaluation, synthesis results were consistently within 5 percent of actual physical implementation results. The tight correlation between synthesis and layout is critical for a predictable RTL-to-GDSII flow," said Richard Busch, director of ASIC Products and Services at IBM Global Engineering Solutions. "We have made topographical technology available in 90nm- and 65nm-based design kits to speed up ASIC design time for our customers."

Design Compiler topographical technology shares technologies with the Galaxy™ Design Platform physical design solution to accurately predict final design results such as timing, area, testability and power during synthesis. It enables RTL designers to foresee results after layout. Using Synopsys' topographical technology-based methodology, IBM's ASIC customers can take corrective measures to ensure that their design will achieve the required performance prior to sending the netlist to IBM for physical implementation. Consequently, IBM receives a better-quality netlist from its customers that speeds up physical implementation while meeting the required performance targets.

"A growing number of ASIC vendors are adopting topographical technology to streamline their design flow," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "IBM's support enables its ASIC customers to reap the benefits of topographical technology in completing their most advanced ASICs much faster, with higher predictability and fewer iterations."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Rachel Modena Barasch
MCA, Inc.
650-325-7547
rbarasch@mcapr.com

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CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or sgulizia@synopsys.com; or Rachel Modena Barasch of MCA, Inc., +1-650-325-7547, or rbarasch@mcapr.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/